

DP8051 Program Memory allocation

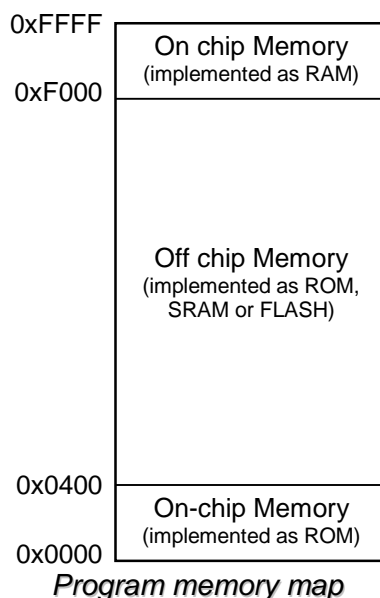
INTRODUCTION

The DP8051 has a program memory interface allowing connection of two memory banks (Internal and External). The size of each Program Memory is fully user configurable. Used interface allows division of the program between each memory bank, as well as implementation of whole program into one of the blocks (Internal or External).

PROGRAM MEMORY ALLOCATION

Program memory space begins from address 0x0000 and ends on 0xFFFF address. After each reset, the CPU starts execution in the program memory at 0x0000 location.

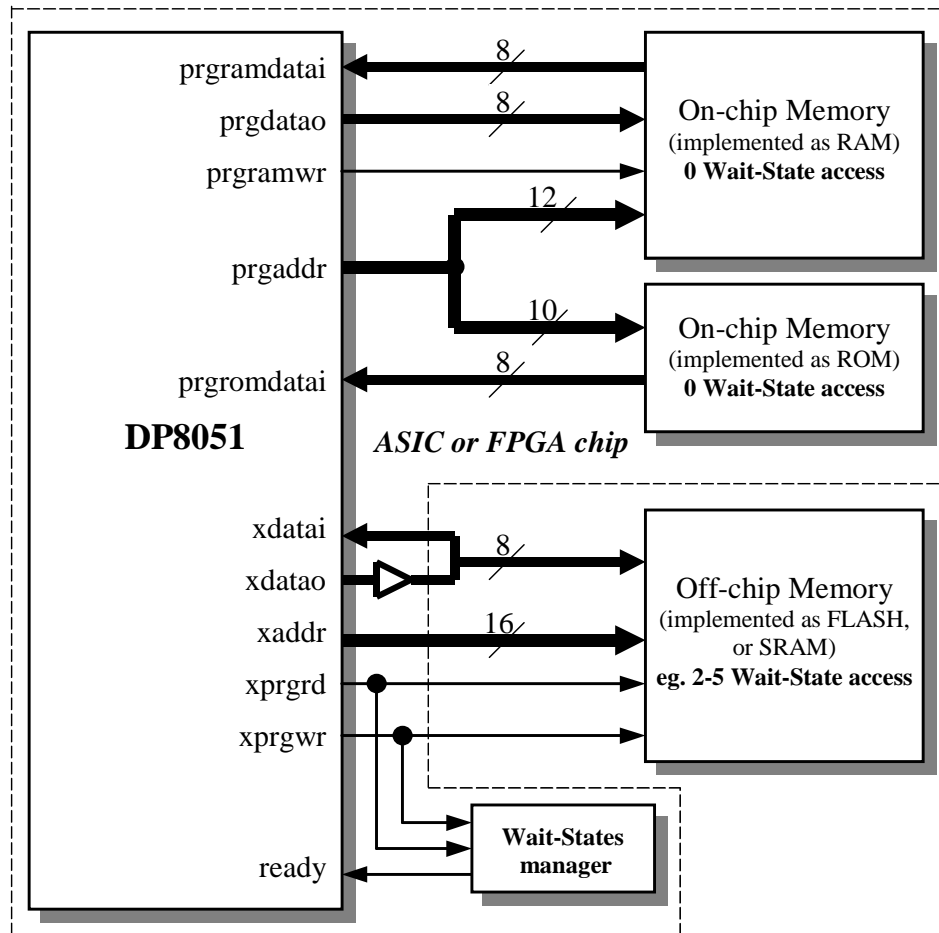
The figure below shows an example Program Memory space implementation in systems with DP8051 Microcontroller core. The On-chip Program Memory located in address space between 0kB and 1kB is typically used for BOOT code with system initialization functions. This part of the code is typically implemented as ROM. The On-chip Program Memory located in address space between 60kB and 64kB is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code during initialization phase from Off-chip memory or through RS232 interface from external device.



The On-Chip program code is executed without wait-states and allow to achieve a top performance up to 200 million instructions per second. (many instructions executed in a single clock cycle).

The Off-chip Program Memory located in address space between 1kB and 60kB is typically used for main code and constants. This part of the code is usually implemented as ROM, SRAM or

FLASH device. Because of relatively long access time to these kind of devices, the program code should be fetched with additional Wait-States. Number of required Wait-States depends on memory access time and DP8051 clock frequency. In most cases the proper number of Wait-States cycles is between 2-5.



Example program memory connections

The described above memory map should be treated as an example. All Program Memory spaces are fully configurable. For timing-critical applications whole program code can be implemented as on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications whole program code can be implemented as off-chip ROM or FLASH and executed with required number of Wait-State cycles.