

DFP2INT

Floating Point To Integer Pipelined Converter

v. 2.20

OVERVIEW

The DFP2INT is the pipelined floating point to integer converter. The input and output numbers format conforms to IEEE-754 standard. DFP2INT supports single precision real numbers and double word integers (4 Bytes). Convert operation is pipelined to 2 levels. Input data are fed every clock cycle. The first result appears after latency equal to 2 clock periods and next results are available each clock cycle. Full precision and accuracy are accomplished.

APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

KEY FEATURES

- Full IEEE-754 compliance
- Single precision real input numbers
- Double word output numbers(4 Bytes)
- Simple interface
- No programming required
- 2 levels pipelining
- Full accuracy and precision
- Results available at every clock
- Overflow, underflow and invalid operation flags

- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - FPGA netlist
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - NCSim automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

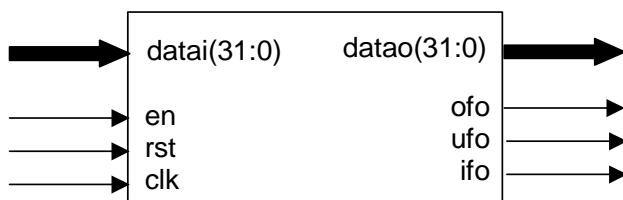
Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	Input	Global system clock
rst	Input	Global system reset
en	Input	Enable computing
dataai[31:0]	Input	Data bus input
dataao[31:0]	Output	Data bus output
ofo	Output	Overflow flag
ufo	Output	Underflow flag
ifo	Output	Invalid result flag

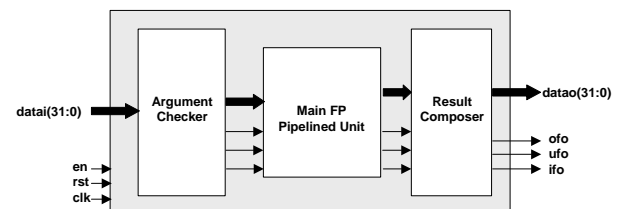
PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route :

Device	Speed grade	Logic Cells	F _{max}
FLEX10KE	-1	335	67 MHz
ACEX1K	-1	335	71 MHz
APEX20K	-1	295	69 MHz
APEX20KE	-1	295	67 MHz
APEX20KC	-7	295	88 MHz
APEX-II	-7	295	114 MHz
MERCURY	-5	270	208 MHz
STRATIX	-5	245	184 MHz
CYCLONE	-6	245	165 MHz
STRATIX-II	-3	185	214 MHz
CYCLONE-II	-6	265	133 MHz

Core performance in ALTERA® devices

BLOCK DIAGRAM



Arguments Checker - performs input data analysis against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given, as the results to the Main FP Pipelined Unit.

Main FP Pipelined Unit - performs floating point to integer conversion. Gives the complex information about the results to Result Composer module.

Result Composer - performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.



CONTACT

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