

DSPI

Serial Peripheral Interface – Master/Slave

v. 2.09

OVERVIEW

The DSPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. DSPI data are simultaneously transmitted and received. What's the most important, it's a technology independent design that can be implemented in a variety of process technologies. The DSPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. It can be configured as a master or a slave device, with data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of eight different bit rates for the serial clock. The DSPI automatically drive selected by SSCR (Slave Select Control Register) slave outputs (SS70 – SS00) and address SPI slave device to exchange serially shifted data. What's more important, error-detection logic is included to support interprocessor communications. A write collision detector indicates, when an attempt is made, to write data to the serial shift register, while a transfer is in progress. A multiple-master mode-fault detector automatically disables DSPI output drivers, if more than one SPI devices simultaneously attempts to become bus

master.

The DSPI is fully customizable, which means, that we deliver it tailored to your configuration and requirements. There is no need to pay extra for not used features and wasted silicon. It includes fully automated testbench with complete set of tests, allowing easy package validation at each stage of SoC design flow.

FEATURES

- SPI Master
 - Master and Multi-master operations
 - 8 SPI slave select lines
 - System error detection
 - Mode fault error
 - Write collision error
 - Interrupt generation
 - Supports speeds up $\frac{1}{4}$ of system clock
 - Bit rates generated $\frac{1}{4}$ - $\frac{1}{512}$ of system clock.
 - Four transfer formats supported
 - Simple interface allows easy connection to microcontrollers
- SPI Slave
 - Slave operation
 - System error detection
 - Interrupt generation
 - Supports speeds up $\frac{1}{4}$ of system clock
 - Simple interface allows easy connection to microcontrollers
 - Four transfer formats supported
- Fully synthesizable, static synchronous design, with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - IP Core updates
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

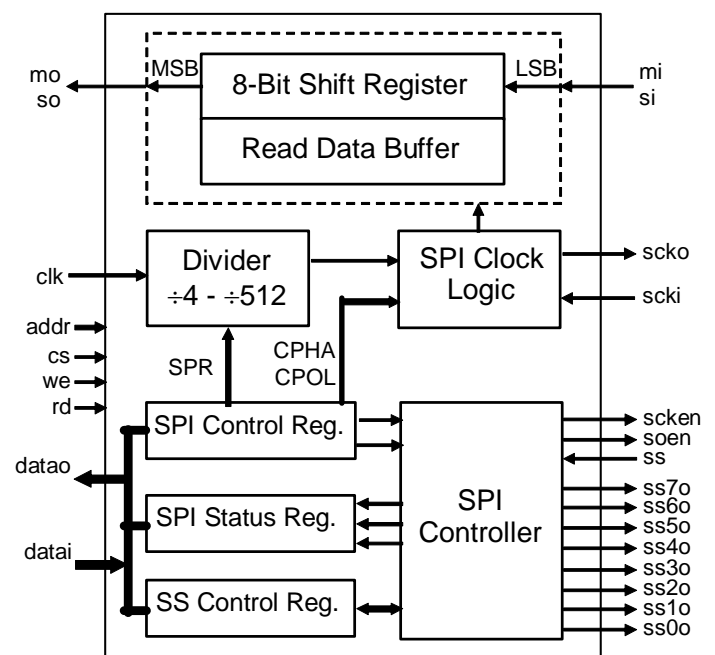
Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

BLOCK DIAGRAM

Shift register and Read Data Buffer – it is a central element in the SPI system. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means, that the new data for transmission cannot be written to the shifter, until the previous transaction is complete; however, received data is transferred into a parallel read data buffer, so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur. When an SPI transfer occurs, an 8-bit character is shifted out on data pin, while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer, is that an 8-bit shift register in the master and another 8-bit shift register in the slave, is connected as a circular 16-bit shift register. When the transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.



Control Register may be read or written at any time, it is used to configure the DSPI System. This register controls the mode of transmission

(Master, Slave), polarity and phase of SPI Clock and transmission speed.

Status Register (SPSR) contains flags, indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence.

Slave Select Control Register configures which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS70-SS00 pins when DSPI master transmission starts.

SPI Clock Logic - Software can select any from four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow master device communication with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.

PERFORMANCE

The following table gives a survey about the Core performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F _{max}
CYCLONE	-6	181	303 MHz
CYCLONE2	-6	172	310 MHz
STRATIX	-5	181	320 MHz

STRATIX2	-3	151	387 MHz
STRATIXGX	-5	181	307 MHz
APEX2A	-7	196	244 MHz
APEX20KC	-7	196	211 MHz
APEX20KE	-1	196	169 MHz
APEX20K	-1	196	135 MHz
ACEX1K	-1	205	156 MHz
FLEX10KE	-1	205	156 MHz
MAX2	-3	181	209 MHz
MAX3K	-5	119	96 MHz
MAX7K	-5	119	96 MHz

Core performance in ALTERA® devices

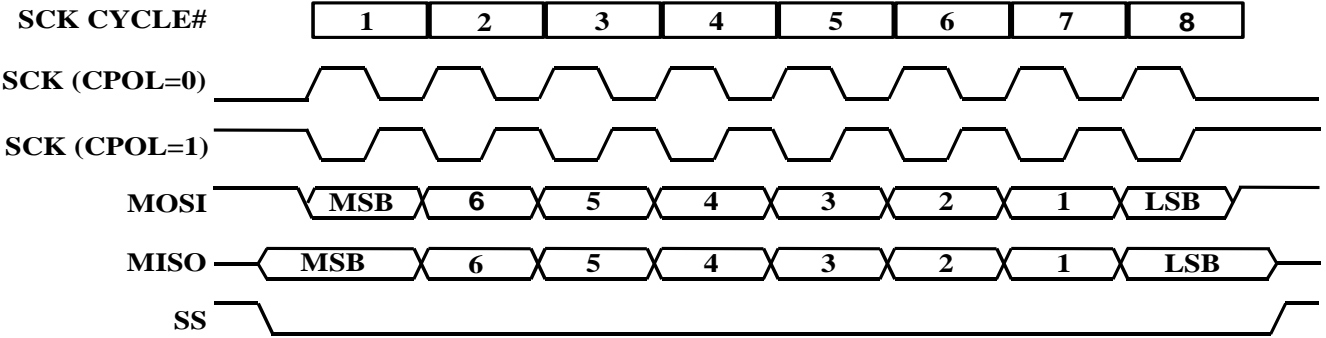
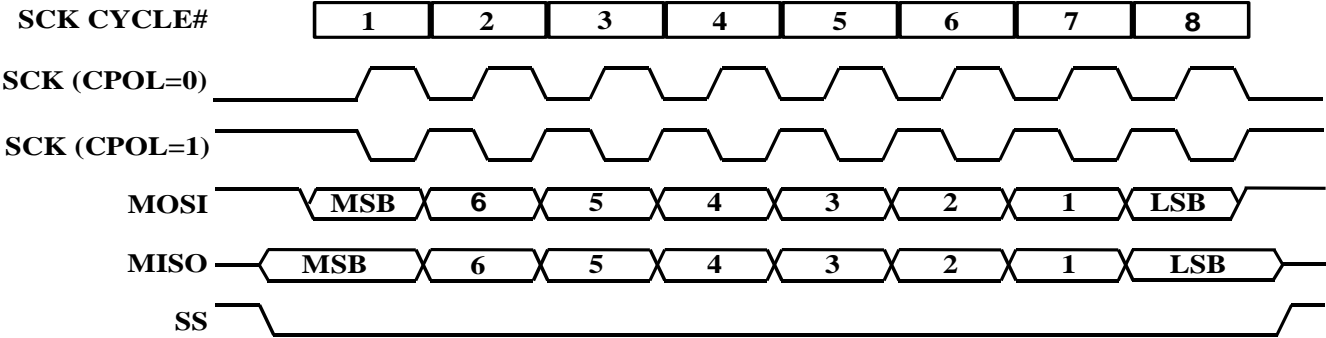
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(7:0)	input	Data bus input
addr(1:0)	input	Processor address lines
cs	input	Chip select
rd	input	Processor read strobe
we	input	Processor write strobe
scki	input	SPI clock input
mi	input	Master serial data input
si	input	Slave serial data input
ss	input	Slave select
datao(7:0)	output	Data bus output
irq	output	Interrupt request
scko	output	SPI clock output
scken	output	SPI clock output enable
mo	output	Master serial data output
so	output	Slave serial data output
soen	output	Slave data output enable
ss7o-ss0o	output	Slave select outputs



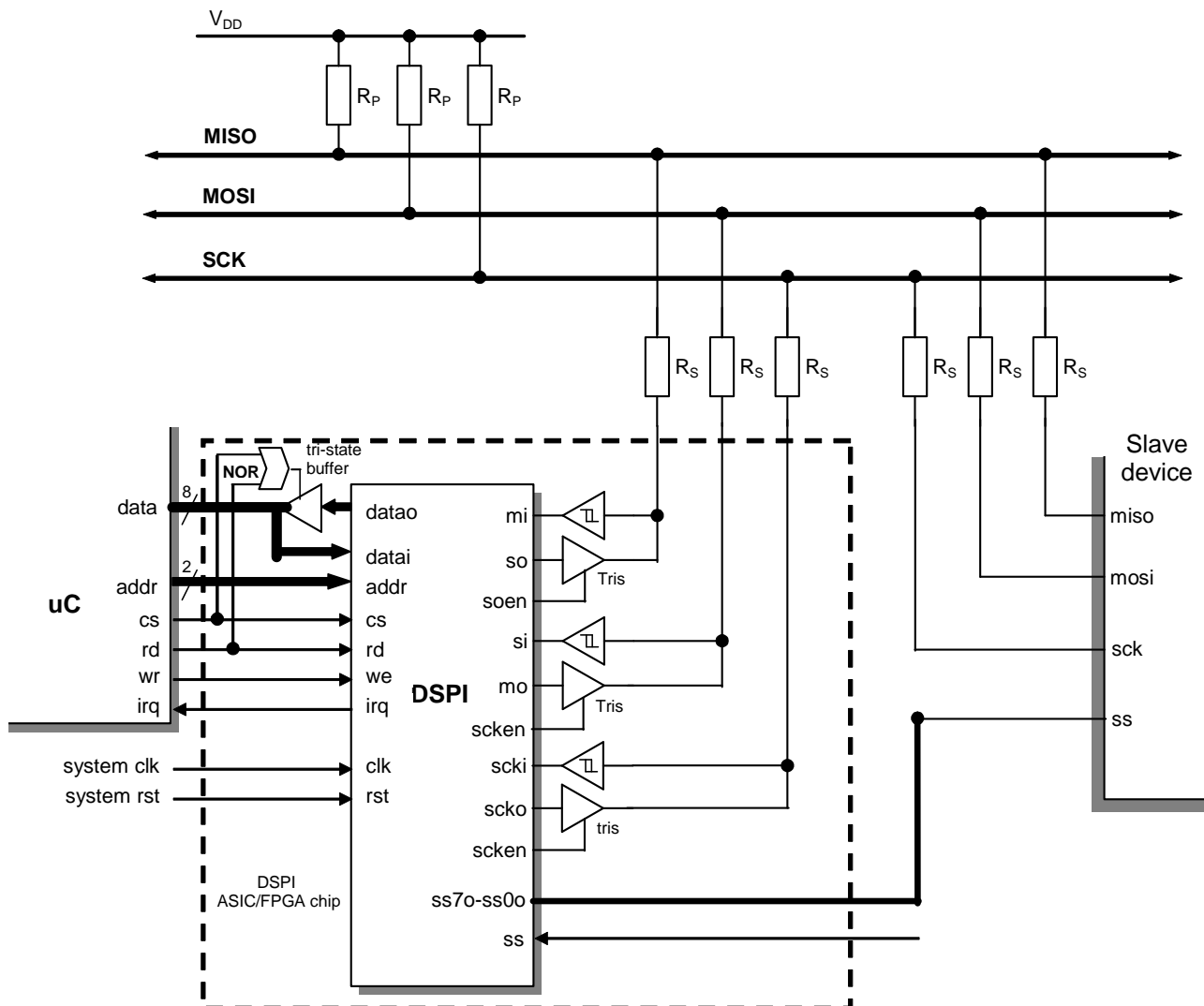
TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit, selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.



TYPICAL uC / BUS CONNECTION

Figure below shows a typical connection the DSPI Core with microcontroller and other SPI Master/Slave devices.



CONTACT

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