

DP8051 performance improvement

1. PERFORMANCE IMPROVEMENT

This document present a speed comparison of DP8051 Core vs. standard 8051 devices. In presented tables are compared numbers of CLK cycles needed to execute selected arithmetic operations. **A 1 cycle is equal to 1 CLK period.**

a) 8-bit addition - immediate data

The following code performs immediate data (constant) addition to an 8-bit register.

$$Rx = Rx + \#n$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
ADD A, #n	24h	2	12	2
MOV Rx, A	F8h-FFh	1	12	1
Sum:			36	4

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b) 8-bit subtraction - direct addressing

The following code performs direct addressing subtraction from an 8-bit register.

$$Rx = Rx - (\text{dir})$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
SUBB A, dir	25h	2	12	2
MOV Rx, A	F8h-FFh	1	12	1
Sum:			36	4

DP8051 Performance Improvement: 9,0

c) 8-bit multiplication

The following code performs the 8-bit registers multiplication.

$$Rx = Rx * Ry$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
MOV B, Ry	88h-8Fh	2	24	2
MUL AB	A4h	1	48	2
MOV Rx, A	F8h-FFh	1	12	1
Sum:			96	6

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d) 8 – bit division

The following code performs the 8-bit registers division.

$$R_x = R_x / R_y$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, R _x	E8h-EFh	1	12	1
MOV B, R _y	88h-8Fh	2	24	2
DIV AB	84h	1	48	6
MOV R _x , A	F8h-FFh	1	12	1
Sum:			96	10

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e) 16 - bit addition

The following code performs 16-bit addition. The first operand and result are located in registers pair RaRb. Second operand is located in registers pair RxRy.

$$R_aR_b = R_aR_b + R_xR_y$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, R _b	E8h-EFh	1	12	1
ADD A, R_y	28h-2Fh	1	12	1
MOV R _b , A	F8h-FFh	1	12	1
MOV A, R _a	E8h-EFh	1	12	1
ADDC A, R_x	38h-3Fh	1	12	1
MOV R _a , A	F8h-FFh	1	12	1
Sum:			72	6

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Performance improvement summary

Total performance improvement of DP8051 vs. standard 8051 devices has been summarized in the table below. It shows the most common used multi-precision arithmetic operation.

Function	80C51 cycle	DP8051 cycle	Improvement
8-bit addition (<i>immediate data</i>)	36	5	9,0
8-bit addition (<i>direct addressing</i>)	36	6	9,0
8-bit addition (<i>indirect addressing</i>)	36	6	9,0
8-bit addition (<i>register addressing</i>)	36	5	12,0
8-bit subtraction (<i>immediate data</i>)	36	5	9,0
8-bit subtraction (<i>direct addressing</i>)	36	6	9,0
8-bit subtraction (<i>indirect addressing</i>)	36	6	9,0
8-bit subtraction (<i>register addressing</i>)	36	5	12,0
8-bit multiplication	96	9	16,0
8-bit division	96	10	9,6
16-bit addition	72	10	12,0
16-bit subtraction	84	11	12,0
16-bit multiplication	312	32	13,6
32-bit addition	144	20	12,0
32-bit subtraction	156	21	12,0
32-bit multiplication	1248	142	12,6
Average speed improvement:			11,12