

# DFPMUL

## Floating Point Pipelined Multiplier Unit

v. 2.70

### OVERVIEW

The DFPMUL uses the **pipelined** mathematics algorithm, to multiply two arguments. The input numbers format is compliant with IEEE-754 standard. DFPMUL supports single precision real number. Multiply operation was pipelined up to 7 levels. Input data are fed every clock cycle. The first result appears after latency, depending on pipeline level and next results are available **each clock** cycle. Full IEEE-754 precision and accuracy were included.

### APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

### KEY FEATURES

- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 7 levels pipeline
- Full accuracy and precision
- Overflow, underflow and invalid operation flags
- Results available at every clock
- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

### DELIVERABLES

- ◆ Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - FPGA netlist
- ◆ VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- ◆ Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

### LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

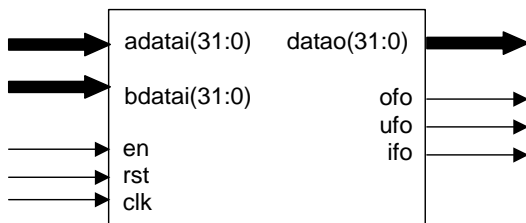
Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used

in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

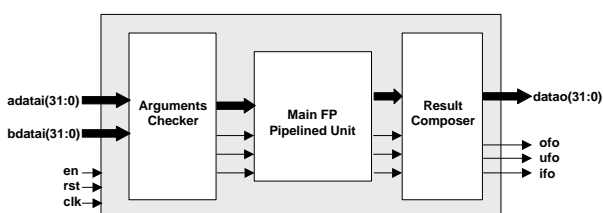
## SYMBOL



## PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	Input	Global system clock
rst	Input	Global system reset
en	Input	Enable computing
adatai[31:0]	Input	A data bus input
bdatai[31:0]	Input	B data bus input
datao[31:0]	Output	Data bus output
ofo	Output	Overflow flag
ufo	Output	Underflow flag
ifo	Output	Invalid result flag

## BLOCK DIAGRAM



**Arguments Checker** - performs input data analysis against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given, as the results to Main FP Pipelined Unit.

**Main FP Pipelined Unit** - performs floating point multiply function. Gives the complex information about the results and makes final flags settings.

**Result Composer** - performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

## PERFORMANCE

The following table gives a survey about the Core area and performance in the ASIC devices :

Device	Optimization	Gates	F <sub>max</sub>
0.25u typical	area	11700	40 MHz
	speed	15900	100 MHz
0.18u typical	area	10600	70 MHz
	speed	14500	150 MHz

*Core performance in ASIC devices*



## CONTACT

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