

# DEEPROM

## Serial EEPROM Controller

ver 1.01

### OVERVIEW

The DEEPROM Controller performs communication and exchanges data between external serial EEPROM Memory and CPU's external memory interface. The serial EEPROM contents is accessible to CPU in the same manner as common SRAM memory, but requires READY input to expand time access.

The Core is designed to operate with popular 25XXX SPI Serial EEPROMs (Atmel, Microchip).

### APPLICATIONS

- Connection of Serial EEPROM to CPU
- Non-volatile data storing

### KEY FEATURES

- Standard memory interface with ready control
- Configurable SPI parameters
  - Serial clock prescaler
  - SPI mode
  - CS hold/setup
- Updating bits in EEPROM status register
- Simple interface allows easy connection to microcontrollers
- Fully synthesizable, static design with no internal tri-states
- Synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan Test ready

### DELIVERABLES

- ◆ Source code:
  - ◇ VHDL Source Code or/and
  - ◇ VERILOG Source Code or/and
  - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench
  - ◇ Active-HDL automatic simulation macros
  - ◇ ModelSim automatic simulation macros
  - ◇ Tests with reference responses
- ◆ Technical documentation
  - ◇ Installation notes
  - ◇ HDL core specification
  - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
  - ◇ IP Core implementation support
  - ◇ 3 months maintenance
    - IP Core updates
    - Delivery the documentation updates
    - Phone & email support

### LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

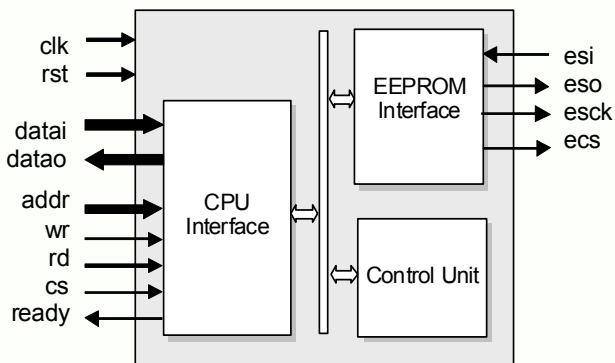
In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

## BLOCK DIAGRAM

**CPU Interface** – Controls access from CPU and generates ready signal control.



**SPI Interface** – Controls serial data transmission based on SPI protocol.

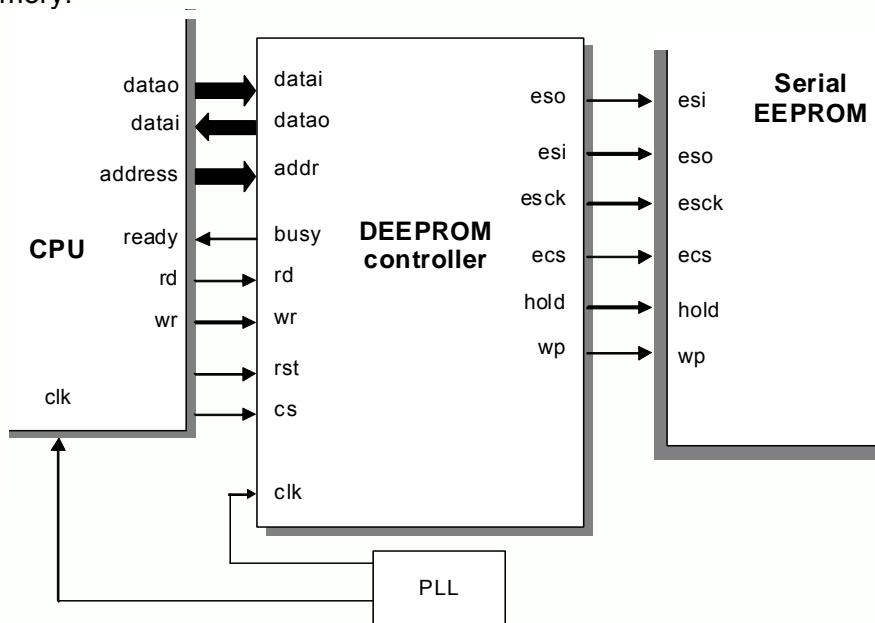
**Control Unit**– Performs main control. Generates commands and data sequences for serial EEPROM device management

## PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
datai(7:0)	input	CPU data bus (input)
addr(15:0)	input	CPU address lines
cs	input	Chip select
rd	input	CPU read strobe
wr	input	CPU write strobe
esi	input	Serial data input
datao(7:0)	output	CPU data bus (output)
ready	output	Data ready control
eso	output	Serial data output
esck	output	Serial clock
ecs	output	Serial device chip select

## TYPICAL DEEPROM CONNECTION

Below is shown typical connection of DEEPROM Controller to microprocessor and serial EEPROM memory.



## CONTACT

For any modification or special request please contact to Digital Core Design or local distributors.

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