

DLCD

LCD/TFT Display Controller

ver 1.10

OVERVIEW

The DLCD is display controller with 24-bit RGB output and synchronization. It may be used for displaying data on LCD or CRT displays. Pixel data has 8-bit resolution and 24-bit RGB output is generated using external LUT with defined color palette. The DLCD is controlled by CPU and uses external memory for data displaying. Display data are accessible for CPU as external data memory. The DLCD is a technology independent design that can be implemented in a variety of process technologies.

APPLICATIONS

- CPU based applications with LCD/TFT or CRT displays

KEY FEATURES

- Maximum resolution 1024x1024
- 24-bit RGB output, 8-bit pixel with external LUT for color palette
- Configurable screen parameters
- Configurable memory data bus width
- Wait states for memory access
- Pixel clock divider
- Display data copying without CPU access
- Display data accessible for CPU as XDATA memory

DESIGN FEATURES

The DLCD IP core is, full synchronous with one clock domain, design. All parameters are configurable by CPU. But there is also capability for setting parameters by modification constants in source file. There is no need to wasting silicon resources for unused features and constant settings.

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ FPGA netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

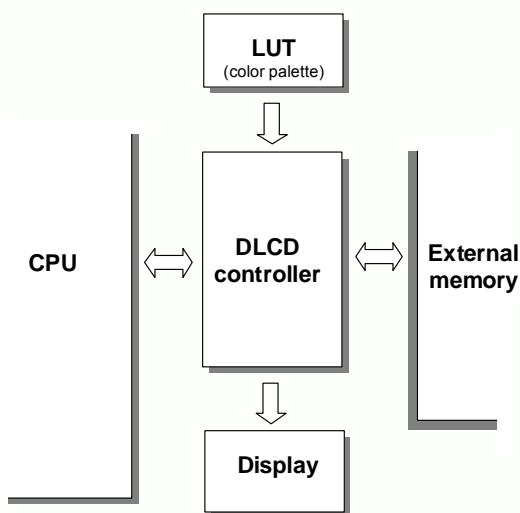
Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

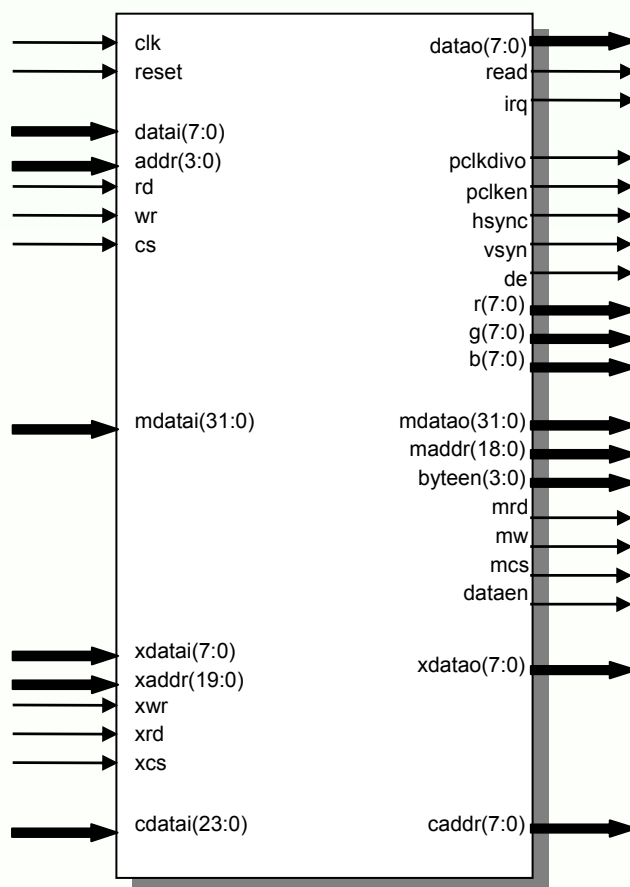
APPLICATION



Typical DLCD and processor connection scheme is shown in figure above.

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SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Master clock
reset	input	Reset
addr(3:0)	input	CPU interface register address
datai(7:0)	input	CPU interface register data input
rd	input	CPU interface register read control
wr	input	CPU interface register write control
cs	input	CPU interface register chip select
xaddr(19:0)	input	CPU interface XDATA address
xdatai(7:0)	input	CPU interface XDATA data input
xrd	input	CPU interface XDATA read control
xwr	input	CPU interface XDATA write control
xcs	input	CPU interface XDATA chip select
mdatai(31:0)	input	Memory data input bus
cdatai(23:0)	input	Color LUT data input bus
irq	output	Interrupt request output
pclkdivo	output	Divided clock output
pcklen	output	Divided Clock enable output
hsync	output	Horizontal synchronization output
vsync	output	Vertical synchronization output
de	output	RGB data valid output
r(7:0)	output	Red color data output bus
g(7:0)	output	Green color data output bus

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

PIN	TYPE	DESCRIPTION
b(7:0)	output	Blue color data output bus
datao(7:0)	output	CPU interface register data output
maddr(18:0)	output	Memory address
mdatao(31:0)	output	Memory data output bus
byteen(3:0)	output	Byte enable control output
mrd	output	Memory read control output
mwr	output	Memory write control output
dataen	output	Memory data output enable
xdatao(7:0)	output	CPU interface XMEM data output
ready	output	Ready control output
caddr(7:0)	output	Color LUT address

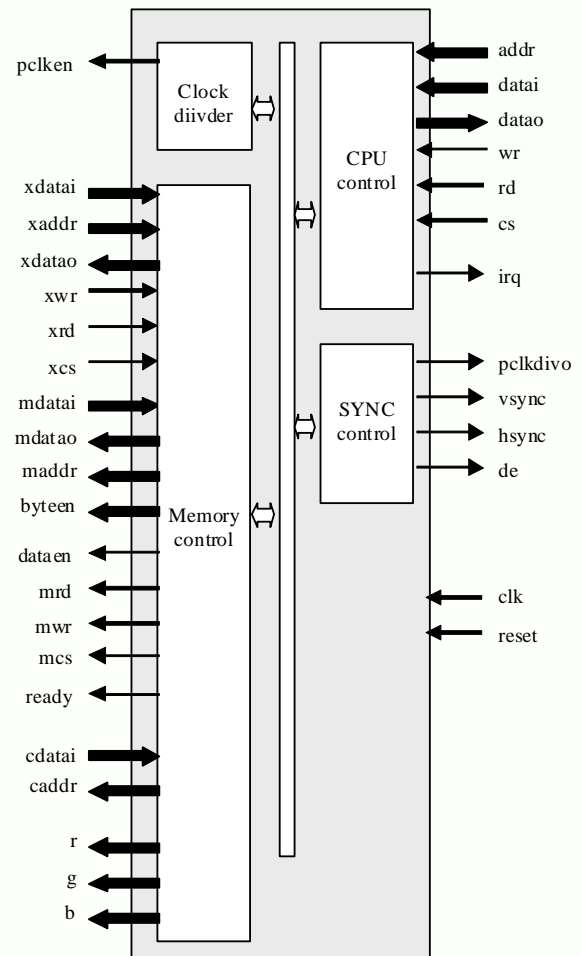
BLOCK DIAGRAM

CPU control – it performs operation of reading and writing internal registers of module.

Sync control – it generates synchronization signals for display and synchronizes data for display.

Memory control – it manages memory access, LUT color palette access, reads pixel data for displaying and controls transactions on external data interface.

Clock divider – it generates divided clock signal for PCLKDIVO output.



CONTACT

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