

DI2CS

I²C Bus Interface - Slave

v. 4.00

OVERVIEW

I²C is a two-wire, bi-directional serial bus, which provides a simple and efficient method of data transmission over short distance, between many devices. The DI2CS core provides an interface between a microprocessor / microcontroller and an I²C bus. It can work as a slave transmitter or slave receiver, depending on working mode, determined by a master device. The DI2CS core incorporates all features required by the latest I²C specification, including clock synchronization, arbitration and High-speed transmission mode. The DI2CS supports all the transmission speed modes.

KEY FEATURES

- Conforms to v.3.0 of the I²C specification
- Slave operation
 - *Slave transmitter*
 - *Slave receiver*
- Supports 3 transmission speed modes
 - *Standard (up to 100 kb/s)*
 - *Fast (up to 400 kb/s)*
 - *Fast Plus (up to 1 Mb/s)*
 - *High Speed (up to 3,4 Mb/s)*
- Allows operation from a wide range of input clock frequencies
- Simple interface allows easy connection to microprocessor/microcontroller devices
- Interrupt generation
- User-defined data setup time
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

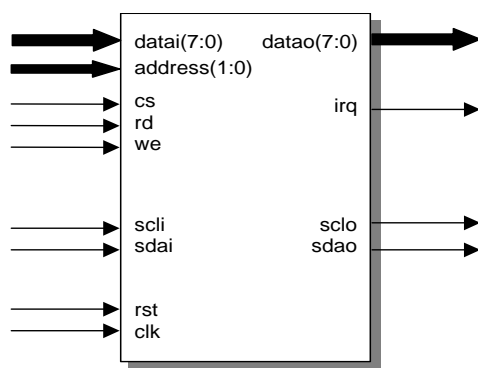
Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL

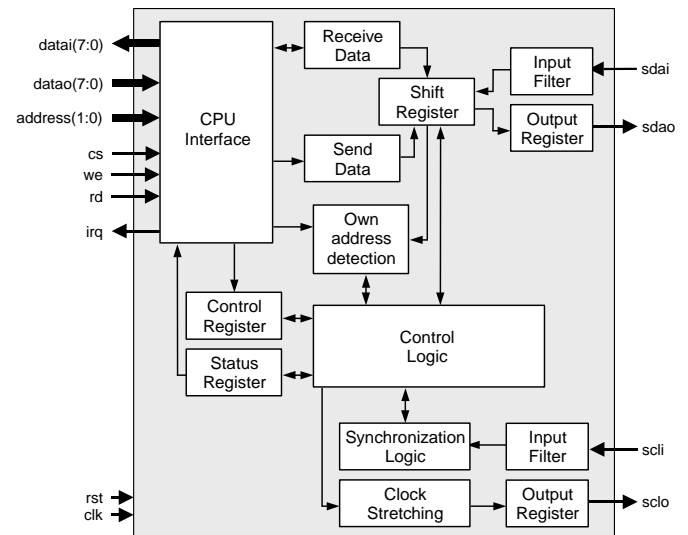


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
address(1:0)	input	Processor address lines
cs	input	Chip select
we	input	Processor write strobe
rd	input	Processor read strobe
scli	input	I ² C bus clock line (input)
sdai	input	I ² C bus data line (input)
dataai(7:0)	input	Processor data bus (input)
datao(7:0)	output	Processor data bus (output)
sclo	output	I ² C bus clock line (output)
sdao	output	I ² C bus data line (output)
irq	output	Processor interrupt line

BLOCK DIAGRAM

Figure below shows the DI2CS IP Core block diagram.



CPU Interface – Performs the interface functions between DI2CS internal blocks and microprocessor. It allows easy connection of the core with the microprocessor/microcontroller system.

Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.

Control Register – Contains five control bits used for performing all types of I²C Bus transmissions.

Status Register – Contains seven status bits, that indicate state of the I²C Bus and the DI2CS core.

Input Filter – Performs spike filtering.

Synchronization Logic – Performs DI2CS core synchronization.

Clock Stretching – Performs I²C SCL clock stretching when DI2CS core is not ready for next transmission.

PERFORMANCE

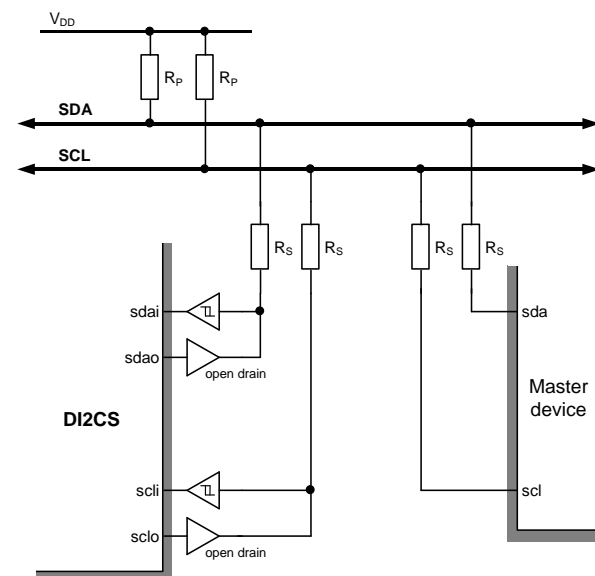
The following table gives a survey about the Core area and performance in the LATTICE® devices after Place & Route (all key features have been included):

Device	Speed grade	LUTs/PFUs	F _{max}
SC	-7	167 / 50	284 MHz
ECP2	-7	183 / 50	245 MHz
ECP2M	-7	153 / 49	258 MHz
XP2	-7	153 / 49	220 MHz
EC	-5	191 / 51	166 MHz
ECP	-5	191 / 51	167 MHz
XP	-5	191 / 51	148 MHz
ispXPGA	-5	147 / 43	141 MHz
ORCA 4	-3	182 / 31	97 MHz
ORCA 3	-7	141 / 31	56 MHz

Core performance in LATTICE® devices

IMPLEMENTATION

Figure below show the typical I2CS implementations in system with Standard, Fast, Fast Plus and High-speed devices.



The main features of each Digital Core Design I²C compliant cores have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application.

Design	I ² C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	Fast Plus Mode	High-speed mode	User defined timing	Spike filtering
DI2CM	3.0	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	3.0	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓	✓
DI2CSB	3.0	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	✓	-	✓
DI2CMS	3.0	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

I²C cores summary table



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