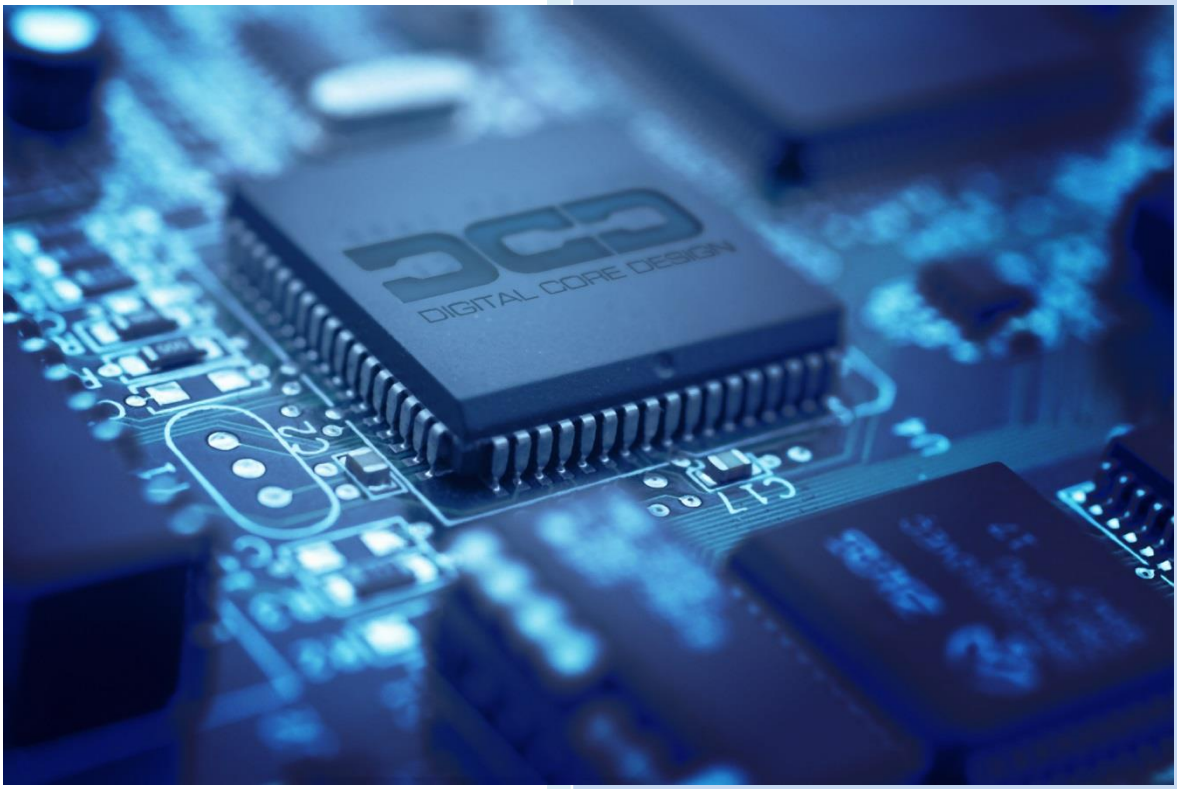
DIGITAL CORE DESIGN

2015

D32PRO IP Core



Deeply Embedded Royalties-Free 32-bit MCU

v. 6.00.preliminary

COMPANY OVERVIEW

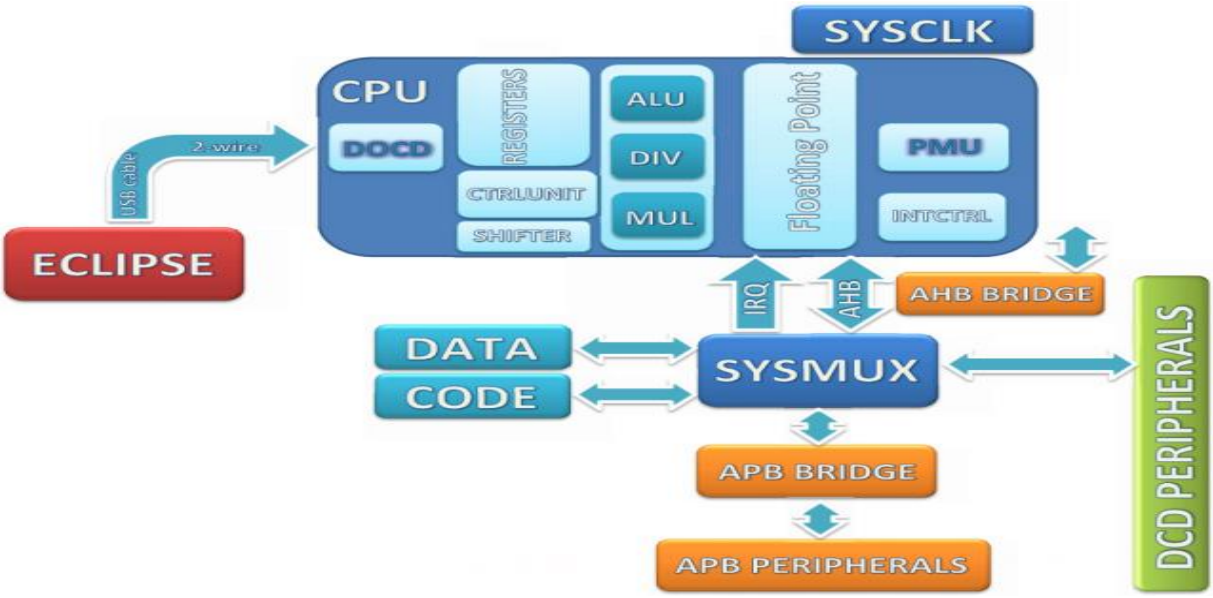
Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we're designing solutions tailored to your needs.

IP CORE OVERVIEW

The D32PRO is **royalty free** **silicon proven**, **high performance** soft core of a single-chip **32-bit embedded controller**, with Floating Point Coprocessor. Thanks to its increased code density, **the D32PRO meets the power and size requirements of new connected devices**. That's why both power and performance of this IP Core predestine it as a real alternative for ARM Cortex M0/M0+/M1/M3 in the **deeply embedded market** and especially for emerging market of connected devices (IoT). Responding to continuing demands for less power drain in system-on-chip (SoC) designs, DCD has developed **an instruction set aimed at reducing the size of a system's instruction memory**. The D32PRO is aimed at low-power always on/always listening systems and those with less demanding clock frequencies such as Bluetooth Low Energy. Nevertheless the core is perfect for **embedded systems that require greater computational performance and system complexity** by supporting dual- and multi-core systems and improved code density. DCD's IP Core is **fully customizable** - it is delivered in the exact configuration to meet customer's requirements. The D32PRO is offered with **great variety of peripherals** like USB, SPI, LCD, HDLC, UART, Ethernet MAC, CAN, LIN, RTC and many more – ready to be implemented with the CPU. The D32PRO is delivered with **fully automated test bench** and complete set of tests, allowing easy package validation at each stage of SoC design.

CPU FEATURES

- ASIC Silicon proven architecture
- Configurable 32-bit Harvard architecture
- 115 Dhrystone MIPS (DMIPS) at @100 MHz
- Small footprint starting at 11k ASIC gates
- Fifteen 32-bit general Purpose registers
- Up to 256 MB of Code Space with encrypted bootloader
- Up to 256 MB of Data Space
- Built-in Floating Point co-processor using dedicated instructions
- Low power consumption by Advanced Power Management Unit
  - *Advanced Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Configurable Interrupt Controller
  - *Non Maskable Interrupt*
  - *Up to 16 priority levels*
  - *Up to 32 external interrupt sources*
- System clock controller supporting
  - *Phase Locked Loops (PLL)*
  - *external clock generator*
  - *on-chip clock oscillator*
- DoCD™ on chip debug unit
  - *Processor execution control*
    - *Run, Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *System Space*
    - *Program Memory Space*
    - *Data Memory Space*
    - *Peripherals Space*
  - *Code execution breakpoints*
    - *up to eight real-time PC breakpoints*
    - *unlimited number of real-time OPCODE breakpoints*
  - *Hardware execution watch-points at*
    - *Data Memory Space*
    - *Program Memory Space*
    - *Peripherals Space*
    - *System Space*
  - *Hardware watch-points activated at a certain*
    - *address by any write into any Space*
    - *address by any read from Space*
    - *address by write into space a required data*
    - *address by read from space a required data*
  - *Hardware watch-point windows activated at a certain*
    - *Start/stop address by any write into any Space*
    - *Start/stop address by any read from Space*
    - *Start/stop address by write into space a required data*
    - *Start/stop address by read from space a required data*
  - *2-wire high-speed communication interface*
- Ultimate dense code
- Great variety of peripherals
- AHB-Lite interface ready
- Rapid & easy development with ready to use tools
- Customization friendly with GUI
- Patent pending architecture
- Royalty free



SOFTWARE DEVELOPMENT PLATFORM

- D32PRO offers Complete Software Development Platform
  - Eclipse Integrated Development Environment
  - *GCC set of tools including C & C++ languages*
  - *Debugger, Linker and Assembler*
  - *Dedicated Simulator*
  - *Supports Linux, Windows*
- Low cost USB debug cable
  - USB2 .0 High Speed cable (480 Mbps)
  - 2-wire high-speed DoCD interface

CONFIGURATION

Several parameters of the D32PRO can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file or using GUI. There is no need to change any parts of the HDL code.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of an IP Core easy and simple.

Single Site license option – dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – dedicated for corporate customers, running their business at several places. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use. There are two formats of the delivered IP Core:

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DELIVERABLES

- ASIC proven architecture
- Source code:
  - VERILOG Source Code or
  - FPGA Netlist
- VERILOG test bench environment
  - ModelSim automatic simulation macros
  - NCSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

CONTACT

For any modifications or special requests, please contact Digital Core Design or local distributors.

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