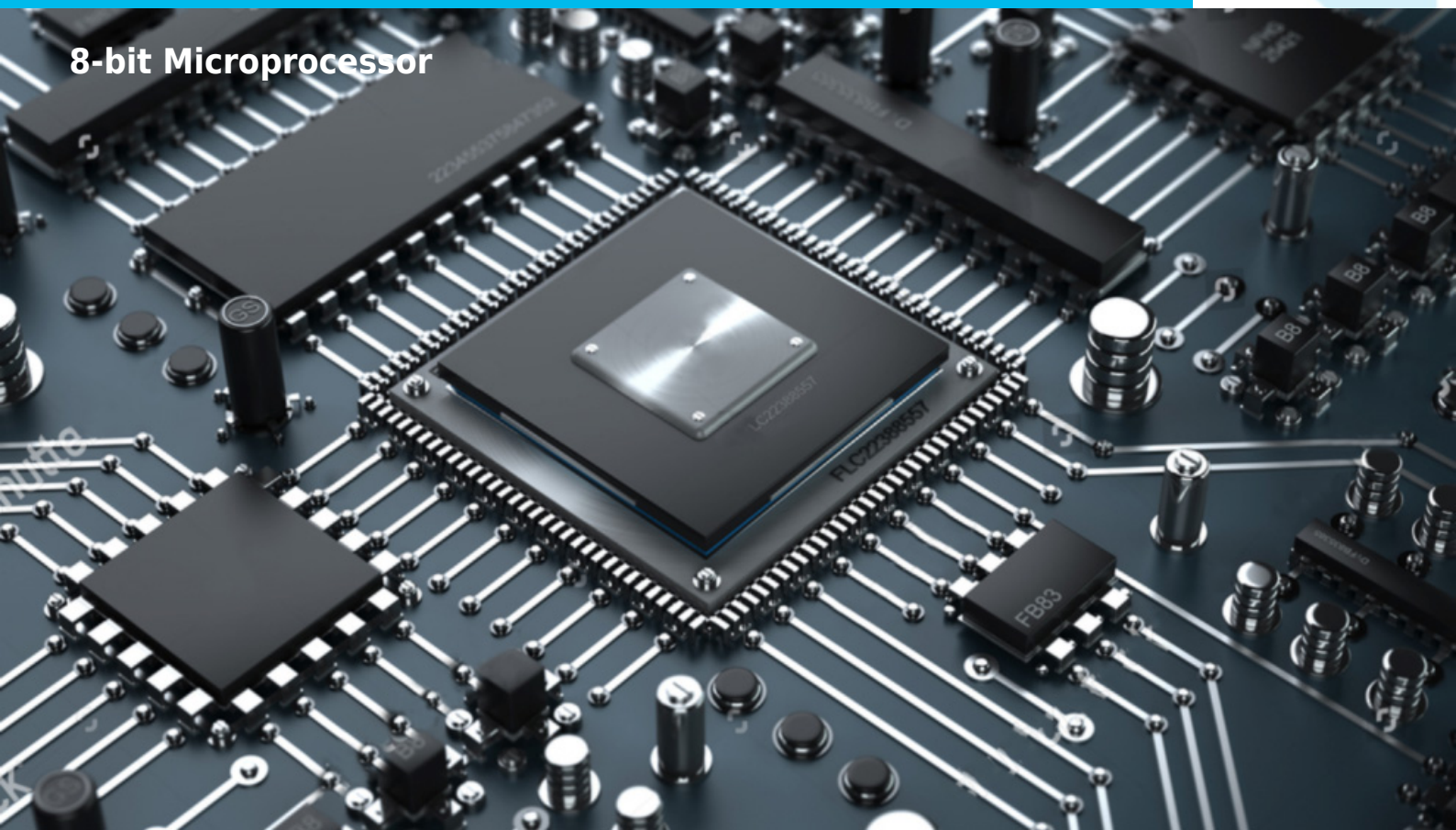
DIGITAL CORE DESIGN

D6802

8-bit Microprocessor



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D6802 is an 8-bit MPU IP Core – synthesizable and fully compatible with the Motorola MC6802. It can be used as **a direct replacement for the MC6802 Microprocessor.** Two software-controlled **power-saving modes** – WAIT and HALT are available to preserve additional power. These modes make the D6802 IP Core especially attractive for **automotive and battery-driven applications**. It is fully customizable – delivered in the exact configuration, to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The D6802 comes with a **fully automated test bench** with a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each DCD's D68XX Core has built-in support for a proprietary Hardware Debug System – **DoCD™**. It is a **real-time hardware debugger** that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of running applications. It can halt, run, step into or skip instruction and read/write any contents of the microprocessor.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

CPU FEATURES

- Cycle compatible with original implementation
- Software compatible with MC6802 industry standard
- De-multiplexed Address/Data Bus, to allow easy memory connection
- Two power saving modes: HALT, WAIT
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages HALT input pin events. **Opcode Decoder** – Performs an instruction opcode decoding and the control functions for all other blocks**. ALU** – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic, like arithmetic unit, logic unit, multiplier and divider. **Bus Controller** – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic. **Interrupt Controller** – The interrupt requests may come from external pins (IRQ and NMI) as well as from particular peripherals. **DoCD™** – Debug Unit – a real-time hardware debugger which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	Speed grade	LE/ALM	Fmax
CYCLONE	-6	1 397	55 MHz
CYCLONE2	-6	1 389	49 MHz
CYCLONE3	-6	1 389	64 MHz
STRATIX2	-3	968	102 MHz

STRATIX3	-2	970	118 MHz
STRATIXGX	-5	1 402	64 MHz
STRATIX2GX	-3	970	99 MHz

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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