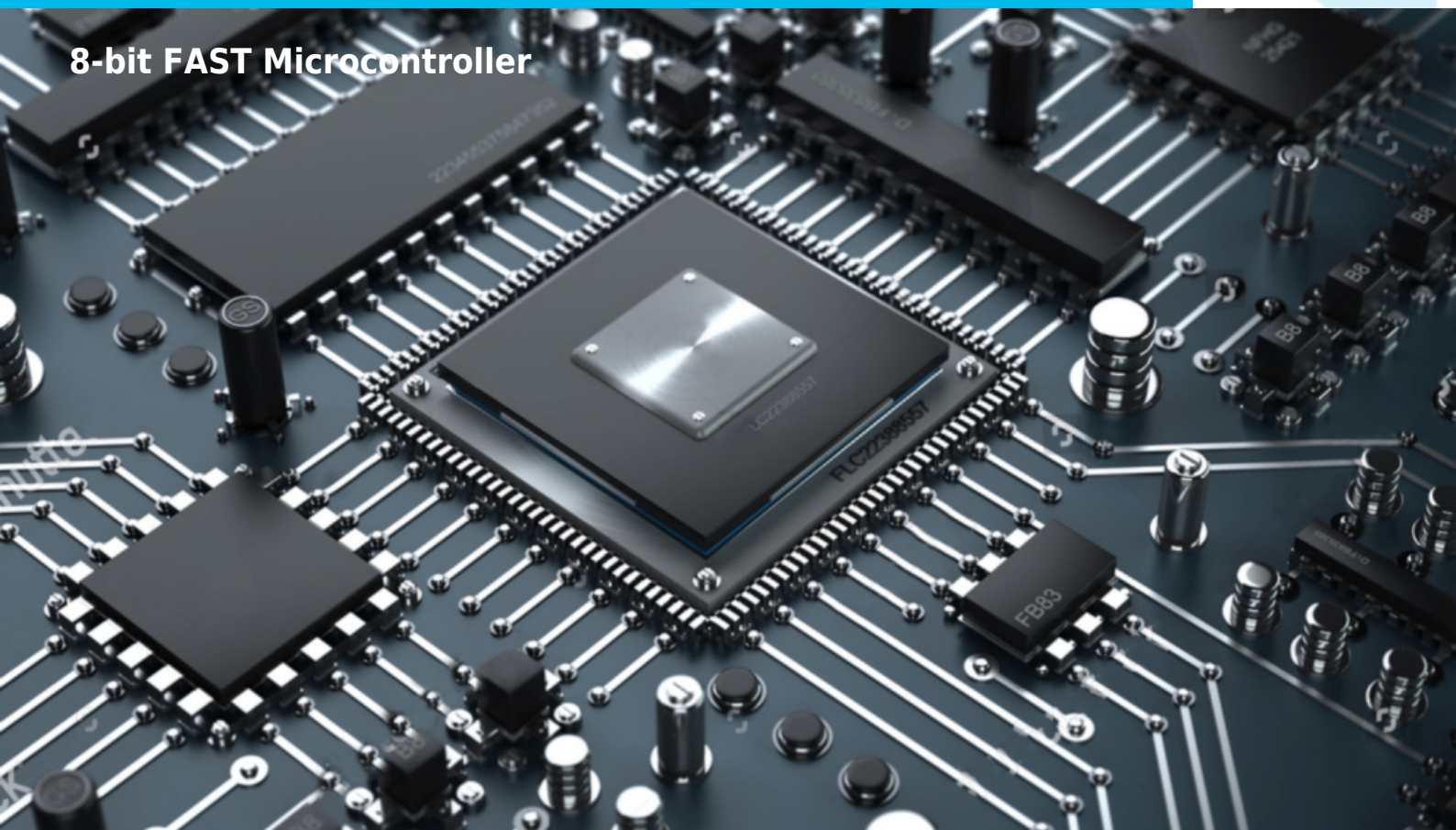
DIGITAL CORE DESIGN

DF6805

8-bit FAST Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DF6805 is an advanced 8-bit MCU IP Core with highly sophisticated, on-chip peripheral capabilities. The DF6805 soft core is **binary-compatible with the industry standard Motorola 68HC05 8-bit microcontroller**. It can achieve performance of **45 – 100 million** instructions per second. The DF6805 has a FAST architecture that is **4.1 times faster** comparing to the original implementation. In the standard configuration the core has major peripheral functions integrated on-chip. The DF6805 Microcontroller Core contains full-duplex UART – Asynchronous Serial Communication Interface (SCI) and can be also equipped with the Synchronous Serial Peripheral Interface (SPI). The main 16-bit, free-running timer system has two input capture lines and two output-compare lines. Self-monitoring circuitry is included on-chip to protect against system errors. The Computer Operating Properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if illegal opcode is detected. Two software-controlled **power-saving modes** – WAIT and STOP are available to preserve additional power. These modes make the DF6805 IP Core especially attractive for **automotive and battery-driven applications**. The DF6805 is **fully customizable** – delivered in the exact configuration to meet your requirements. There's no need to pay extra for unused features and wasted silicon. It includes **fully automated test bench** with **complete set of tests**, allowing easy package validation at each stage of SoC design flow. Each DCD's DF68XX Cores has a built-in support for a proprietary Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger** which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides a **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, SFRs, including user defined peripherals, data and program memories.

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

CPU FEATURES

- FAST architecture – **4.1 times faster** than the original implementation
- Software compatible with 68HC05 industry standard
- 11 times faster multiplication
- 64 bytes of System Function Registers space (SFRs)
- Up to 64K bytes of Data Memory
- Up to 64K bytes of Code Memory
- De-multiplexed Address/Data Bus to allow easy memory connection
- Two power saving modes: STOP, WAI
- Ready pin allows Core to operate with slow program and data memories.
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Positive edge clocking and no internal tri-states
- Scan test ready
- **1 GHz** of virtual clock frequency compared to original implementation
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

The peripherals listed below are implemented in standard configuration of DF6805.

- **DoCD™ On-Chip Debugger**
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
  - Three wire communication interface
- **Four 8-bit I/O Ports**
- **Interrupt Controller**
  - 7 interrupt sources
  - 7 priority levels
  - Dedicated Interrupt vector for each interrupt source
- **Main16-bit timer/counter system**
  - 16 bit free running counter
  - Timer clocked by internal source
- **16-bit Compare/Capture Unit**
  - Two independent input-capture functions
  - Two output-compare channels
  - Events capturing
  - Pulses generation
  - Digital signals generation
  - Gated timers
  - Sophisticated comparator
  - Pulse width modulation
  - Pulse width measuring
- **Full-duplex UART – SCI**
  - Standard Non-return to Zero format (NRZ)
  - 8 or 9 bit data transfer
  - Integrated baud rate generator
  - Noise, Overrun and Framing error detection
  - IDLE and BREAK characters generation
  - Wake-up block to recognize UART wake-up from IDLE condition

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- Three SCI related interrupts

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DF6805 Core) are also available. The optional peripherals can be implemented upon customer's request.

- **ADC – support**
- **I2C bus controller – Master**
- **I2C bus controller – Slave**
- **PWM – Pulse Width Modulation Timer**
- **Fixed-Point arithmetic coprocessor**
- **Floating-Point arithmetic coprocessor IEEE-754 standard single precision**

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and wakes-up the processor from the STOP mode.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks**.**
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A), Condition Code Register (CCREG), Index registers (X) and related logic like arithmetic unit, logic unit and multiplier.
Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface – controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register and related logic.
Interrupt Controller – DF6805 extended IC has implemented 7-level interrupt priority control. The interrupt requests may come from external pin (IRQ), as well as from particular peripherals. The DF6805 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized, according to default arrangement established during reset. When interrupt condition occurs, an interrupt status flag is set, to indicate the condition.
I/O Ports – All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD, to control ports data flow. It assures that all DF6805's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output, then data registers are driven out of those pins. Reads from port pins configured as input, causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins, not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.
Timer & Compare – The programmable timer is based on free-running 16-bit counter, with a fixed divide by four prescaler, plus input capture/output compare circuitry. The timer can be used for many purposes, including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and low byte of that functional block. Accessing the low byte of a specific timer function, allows full control of that function, however, an access of the high byte inhibits that specific timer function, until the byte is also accessed. Each of the input-capture channel has its own 16-bit time capture latch (input-capture register) and each of the output-compare channel, has its own 16-bit compare register. Additional control bits permit software to control the edge(s) that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although for some specific timing applications, it is not as efficient, as a dedicated hardware.
Watchdog Timer – Consist of a free running Timer CLK/2^{13} and control logic. The Watchdog Timer can be enabled by software, by writing '1' to the WDOG bit in MISC register ($000C). Once enabled, the WDT Timer cannot be disabled by software. In addition, the WDOG bit acts as a reset mechanism for the WDT Timer. Writing logic one '1' to the WDOG bit clears Watchdog counter and inhibits Watchdog timeout.
SCI – a full-duplex UART type, asynchronous system, using standard non return to zero (NRZ) format: 1 start bit, 8 or 9 data bits and a 1 stop bit. The DF6805 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate, between the sending device and the SCI, are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. For the start and stop bits, seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability, to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication, that can be used in applications with a modem.
DoCD™ – Debug Unit – it's a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as

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well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX®** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
SPARTAN- II	-6	1 169	38 MHz
SPARTAN-IIE	-7	1 167	40 MHz
SPARTAN-III	-5	1 164	49 MHz
SPARTAN-IIIE	-4	1 195	37 MHz
VIRTEX	-6	1 173	36 MHz
VIRTEX-E	-8	1 171	42 MHz
VIRTEX-II	-6	1 165	77 MHz
VIRTEX-IIP	-7	1 160	87 MHz
VIRTEX-IV	-12	1 183	100 MHz

The area utilized by each unit of the DF6805 core in vendor specific technologies is summarized in the following table.

Component	Area	
	[Slices]	[FFs]
CPU*	669	153
Main Timer	80	55
COM/CAP	90	60
Watchdog	31	14
UART – SCI	214	124
I/O Ports	81	64
Total area	**1 165**	**470**

*CPU – consisted of ALU, Control Unit and Instruction Decoder, Bus Controller with support for 64KB RAM, External IRQ pin Interrupt Controller.

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Transparent and clearly defined licensing methods without royalty-per-chip fees, make use of our IP Cores easy & simple.
– ***Single-Site license option*** – dedicated to small and middle sized companies, which run their business in one place.
– ***Multi-Site license option*** – dedicated to corporate customers who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
– VHDL or Verilog RTL synthesizable HDL Source code
– FPGA EDIF/NGO/NGD/QXP/VQM Netlist

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