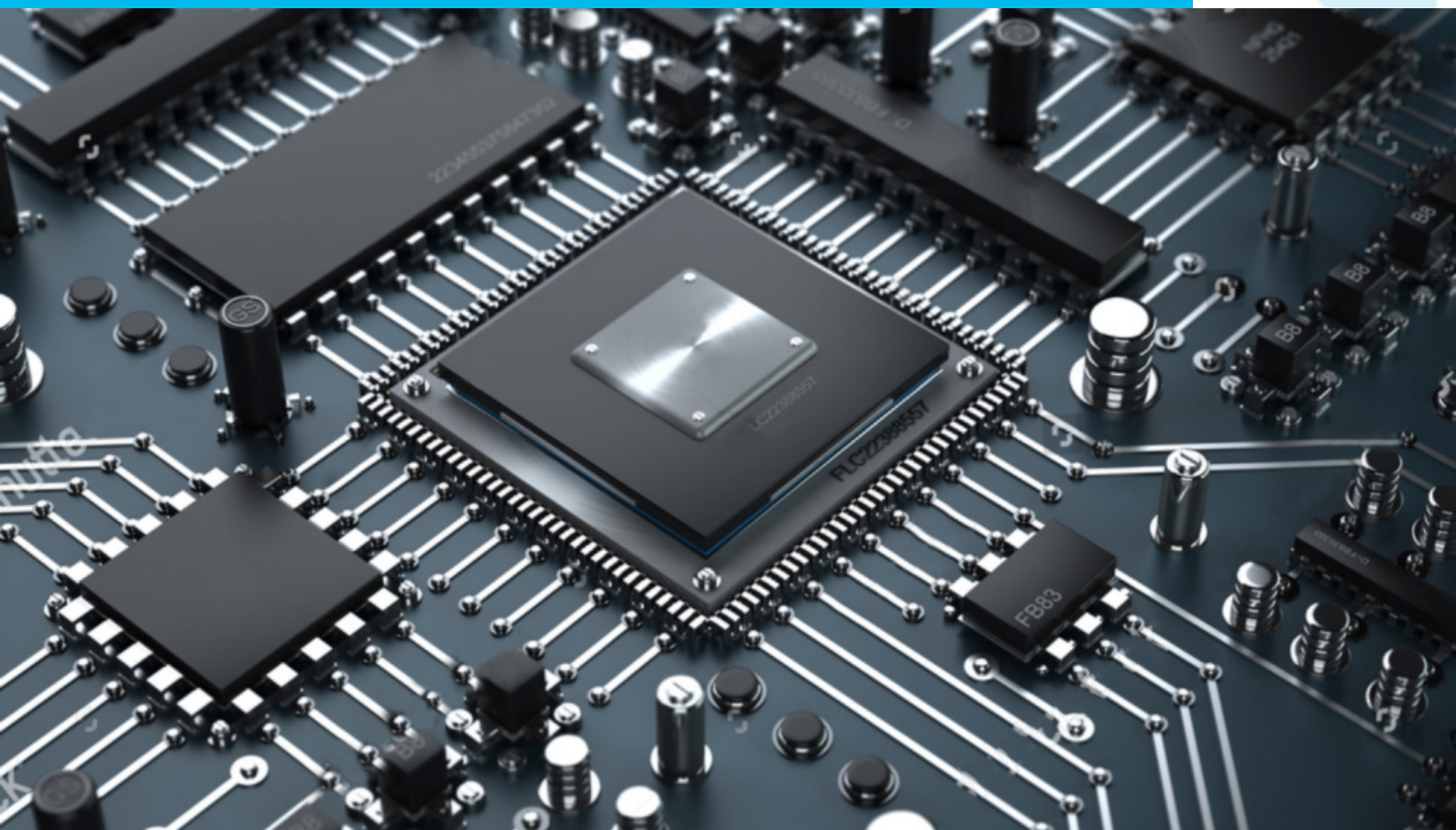
DIGITAL CORE DESIGN

DOCD – DCD ON CHIP DEBUGGER



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The future is now... Digital Core Design believes in Power of Innovation. Thanks to our revolutionary on-Chip Debugger, you can easily become a part of that innovation. The **DoCD™** is a complete debugging system, dedicated for DCD's DQ80251 / DQ8051 / DT8051 / DP8051x / DP80390x Microcontroller Cores. The system consists of three major blocks:

- **Debug IP Core**
- **Hardware Assisted Debugger**
- **Debug Software**

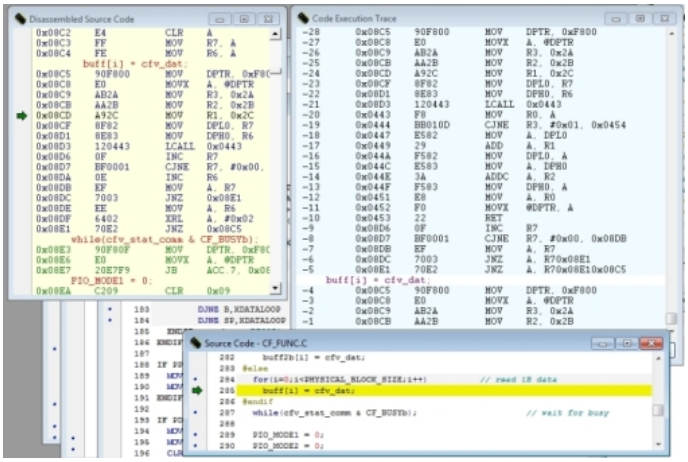
DoCD™ provides some serviceable features, like a **real-time** and **non-intrusive** debug capability, enabling a pre-silicon validation and post-silicon and on-chip software debugging. It allows hardware breakpoints, trace, variables watch and multi C sources debugging. The **DoCD™** Debug Software can work as a ***hardware debugger***, as well as ***software simulator*** – some tasks can be validated at software simulation level and after this step, you can continue real-time debugging by uploading the code into silicon.

As a **DoCD™** user you've got a freedom of choice – you can choose your favourite C compilers or assemblers for software development – it supports most of High Level Object files produced by C/ASM compiler tools:

- Extended OMF-51 produced by Keil compiler
- IAR EWB 8051 & 80390 workbench
- OMF-51 produced by Tasking compiler
- Standard OMF-51 produced by some 8051 compilers
- Extended OMF-251 produced by Keil compiler
- NOI format file produced by SDCC-51 compiler
- Intel HEX-51 format produced by each 8051 compiler
- Intel HEX-386 format produced by each 80390 & 80251 compiler
- BIN format produced by each 8051 & 80390 & 80251 compiler

Instruction Smart Trace

The **DoCD™** Hardware Debugger provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the DoCD™ provides non-intrusive debugging of a running application. It can also efficiently save designer's time thanks to a **hardware trace** called **Instructions Smart Trace buffer (IST)**. The DoCD-IST **captures instructions in a smart and in non-intrusive way**, so it doesn't capture addresses of all executed instructions, but only those related to the start of tracing, conditional jumps and interrupts. This method does not only **save time**, but also allows to **improve the size of the IST buffer and extend the trace history**. Captured instructions are read back by the DoCD debug software, analysed and then presented to the user as an ASM code and related C lines.



Perfect service for free

The reason for the development of the **DoCD™** was to provide our customers with the ability of easy system verification and software debugging, at no additional charges. Therefore, we have decided to add **the complete debug system** to each 8051/80251/80390 IP Core – **for free.** Now DCD's customers have the exceptional possibility to obtain **the complete solution** for making their own 8051/80251/80390 based, SoC, with the ability of pre-silicon validation and post-silicon software debugging **in one place**. It's really an unusual opportunity for the designer to have the ability to get a **high quality IP Core** and **unique on-chip debug tool** from the same supplier.

DOWNLOAD THE DoCD

GO BEYOND THE LIMITS

System-on-Chip designs are facing the problem of inaccessibility of important control and bus signals, because they often lay behind the physical pins of the device – that makes traditional measurement instrumentation useless. The best way to get around those limitations, is to use on-chip debug tools for the tasks verification and software debuging. Other advantage of an on-chip debugger, is its improved

design productivity in an integrated environment, with graphical user's interface. Ability to display/modify memories' content, processor's and peripherals' register windows, along with information tracing and ability to see the related C/ASM source code, are the key elements, that help to improve the design process and thereby, to increase productivity.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– ***Single-Site license option*** – dedicated to small and middle sized companies which run their business at one place.

– ***Multi-Site license option*** – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited.

There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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