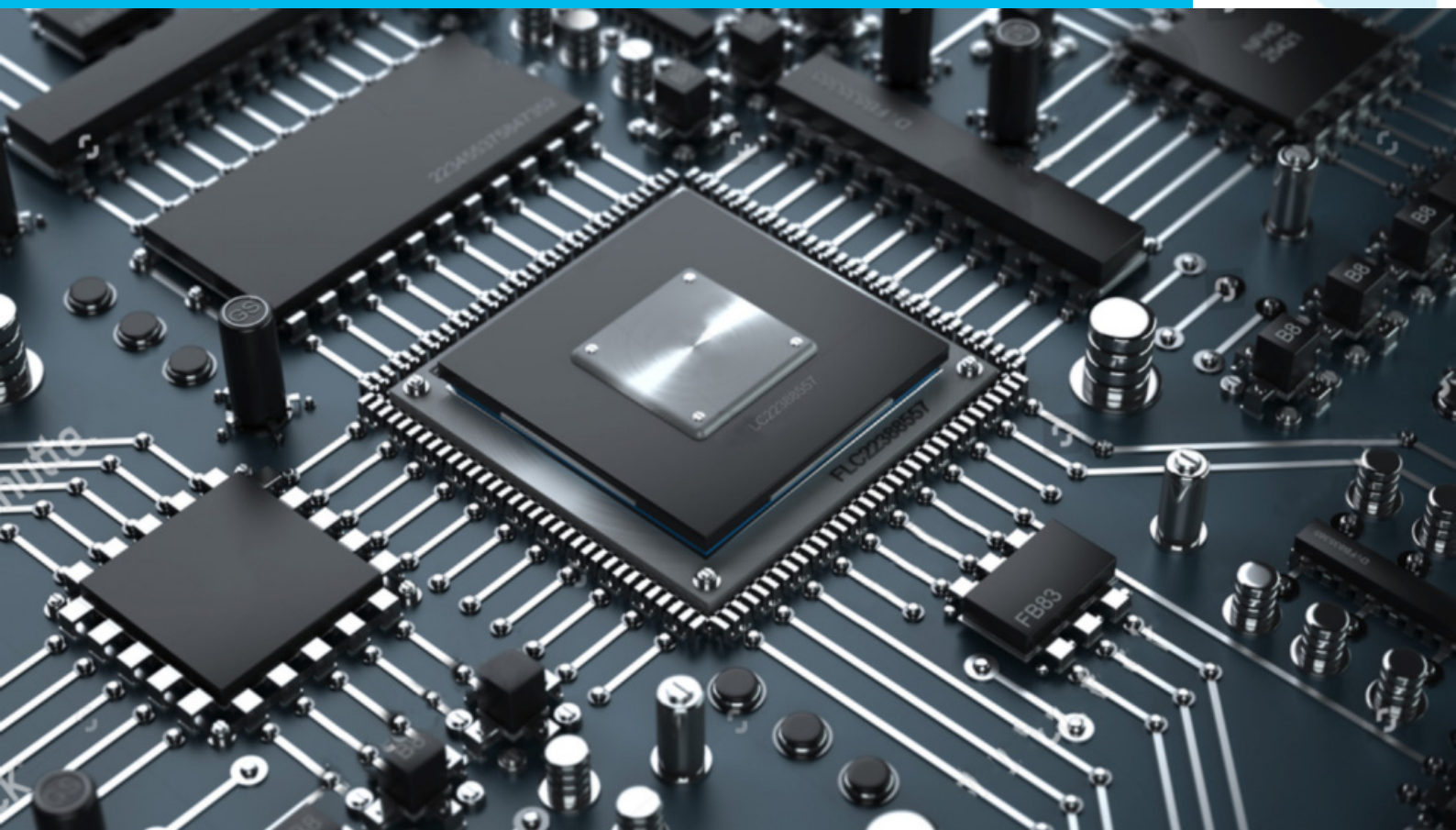
DIGITAL CORE DESIGN

D68XX DOCD – DCD ON CHIP DEBUGGER



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

Join to our team and improve your design skills. IP Core implementations have never been easier before. Thanks to the D68XX **DoCD™** you get a complete debugging system, dedicated for DCD's Motorola compatible D68XX Microprocessors and Microcontroller IP Cores. The system supports all 68XX Cores offered by DCD. The D68XX DoCD™ provides **real-time** and **non-intrusive** debugging capability, enabling pre-silicon validation and post-silicon, on-chip software debugging. The system consist of three major blocks:

- **Debug IP Core**
- **Hardware Assisted Debugger**
- **Debug Software**

The **DoCD™** allows hardware breakpoints, trace, variables watch, multi C sources debugging. The D68XX **DoCD™** Debug Software can work as a ***hardware debugger***, as well as ***software simulator*** – some tasks can be validated at software simulation level and after this step, you can continue real-time debugging by uploading the code into silicon.

As a D68XX **DoCD™** user, you can use your favorite C compilers or assemblers for software development – it supports most of **High Level Object** files produced by C/ASM compiler tools:

- **S19 HEX files**
- **INTEL HEX files**
- **ELF/DWARF 2.0.0.**
- **IAR UBROF**

Go beyond the limits

System-on-Chip designs are facing the problem of inaccessibility of important control and bus signals, because they often lay behind the physical pins of the device – that makes traditional measurement instrumentation useless. The best way to get around those limitations is to use on-chip debugging tools for the tasks verification and software debugging. Other advantage of an on-chip debugger is the improved design productivity in integrated environment with graphical user interface. The ability to display/modify memories' content, processor's and peripherals' register windows, along with information tracing and ability to see the related C/ASM source code, are the key elements that help to improve the design process and thereby, to increase productivity.

Perfect service for free

The reason for development of the **DoCD™** was to provide our customers with the ability of easy system verification and software debugging, at no additional charges. Therefore, we have decided to add **the complete debug system** to each D68XX IP Core – **for free**. Now DCD's customers have the exceptional possibility to obtain the complete solution for making their own D68XX based SoC, with the ability to pre-silicon validation and post-silicon software debugging **at one place**. It's really an unusual opportunity for the designer to have the ability to get a high quality IP Core and unique on-chip debugging tool from the same supplier.

DOWNLOAD THE DoCD

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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