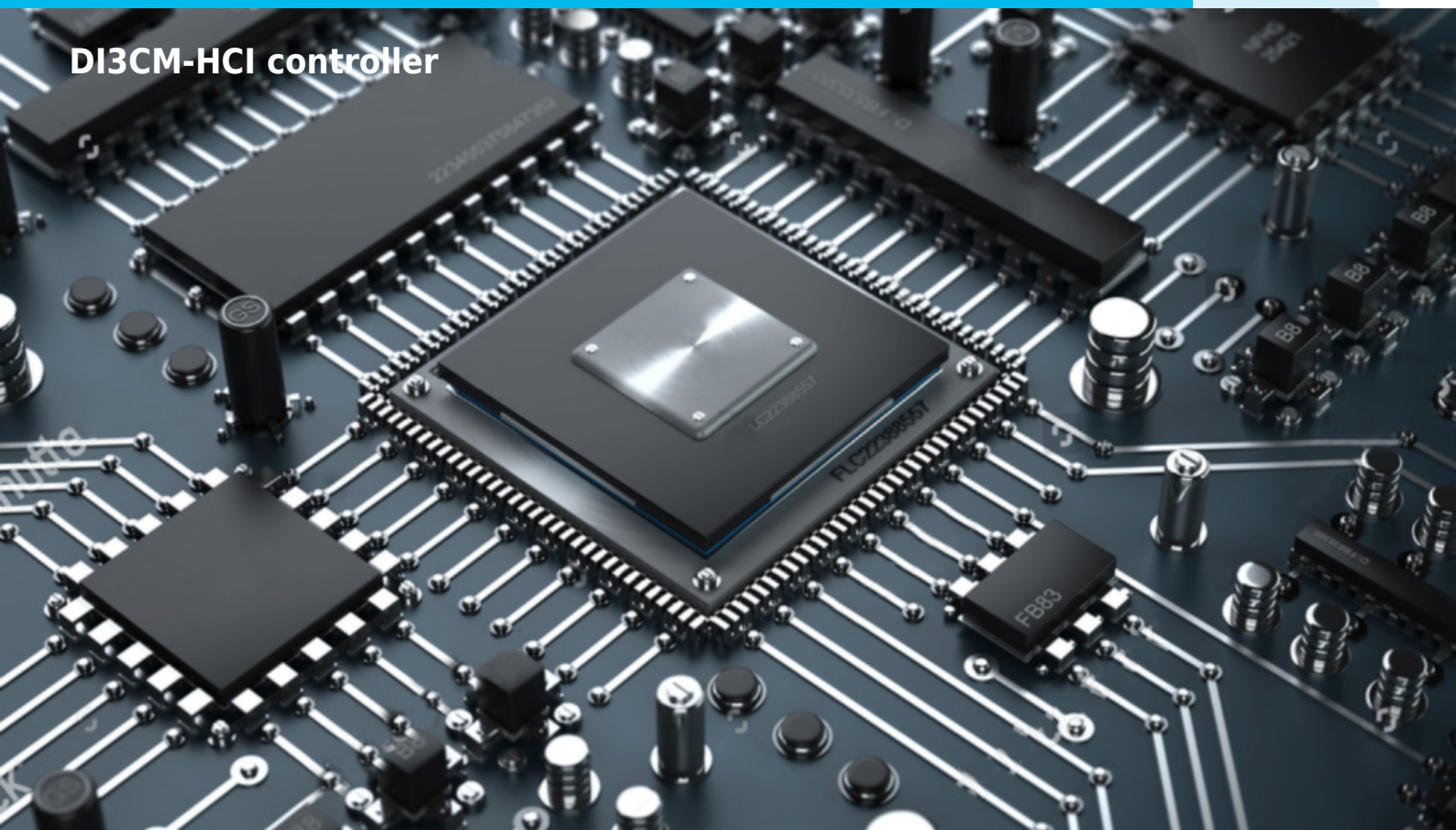
DIGITAL CORE DESIGN

DI3CM-HCI



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The I3C (Improved Inter-Integrated Circuit) is the successor of the I2C bus. Keeping the best assets from its elder brother, the I3C has major improvements in use and power, and performance. The Core uses just two pins and consumes a fraction of the energy, reducing cost and complexity while allowing multiple sensors from different vendors to be easily interfaced with a controller or application processor.

DCD maintains backward compatibility, enabling a smooth transition from I2C to I3C and simple implementation. The newest Core offers a flexible multi-drop interface between a host processor and peripheral sensors, to support the growing usage of sensors in embedded systems. The same I3C standardizes sensor communication, reduces the number of physical pins used in sensor system integration, and supports low-power, high-speed, and other critical features that are currently covered by I2C and SPI.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Conforms to MIPI I3C v1.1 specifications
- **MIPI Manufacturer ID: 0x03B3**
- Dynamic Addressing while supporting Static Addressing for Legacy I^2C Devices
- Legacy I^2C messaging
- I^2C-like Single Data Rate messaging (SDR)
- Master operation with FIFO:
  - *Master transmitter*
  - *Master receiver*
- Supports flexible transmission speed modes:
  - *FAST-PLUS (up to 1000 kb/s)*
  - ***SDR (up to 12,5 Mb/s)***
- **Configurable FIFO size up to 256 Bytes**
- **Configurable SDA/SCL glitch filter**
- **Software programmable SDA/SCL bus timings**
- Multi-master systems supported
- Interrupt generation
- Allows operation from a wide range of input clock frequencies (build-in 12-bit clock timer)
- Configurable interface allows easy connection to standard bus interfaces: APB, AHB, 8051, 80251, others
- Support for in-band interrupts
- Support for I3C common command codes
- Dynamic address assignment (DAA) support
- Command queue support
- Low power management support
- Fully interoperable with third-party I3C master and slave solutions
- Fully synthesizable, static synchronous design with positive edge clocking and synchronous reset
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

DELIVERABLES

- Source code:
  - VERILOG Source Code
  - VERILOG test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

APPLICATIONS

The I3C was initially intended for mobile applications as a single interface that can be used for any sensor. Modern smartphones that include a multitude of sensors and a slew of supporting logic lines are pushing the boundaries of both I^2C and SPI. That's why I3C accommodates many sensors on the

same communication bus, while eliminating additional logic signals needed to support interrupt or sleep mode functionality. Of course, The DI3CM-HCICore is useful for other applications than smartphones. It offers high speed data transfer at very low power levels, which is highly desirable for any embedded system. One of the examples are wearables (where multiple sensors are used in a very limited physical space and with stringent power restrictions). And if it's not enough it's worth to mention that DCD's IP Core as a standardized sensor interface can be utilized as a bus communication standard for touch sensing, always-on and low resolution cameras, acoustics, environmental sensors and transducers that currently use I²C, SPI, UART and others:

- Smartphones, tablets and laptops,
- IoT,
- Medical, health & fitness,
- Autonomous vehicles and ADAS,
- Embedded microprocessor boards,
- Low-power applications,
- Communication systems etc.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route of exemplary devices:

Device		
Cyclone V	1374 ALMs	1063 Regs
Max 10	3010 LEs	919 Regs
Stratix V	1379 ALMs	1005 Regs

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/