DIGITAL CORE DESIGN

DI3CM-HCI – MIPI® I3C CONTROLLER (MASTER)

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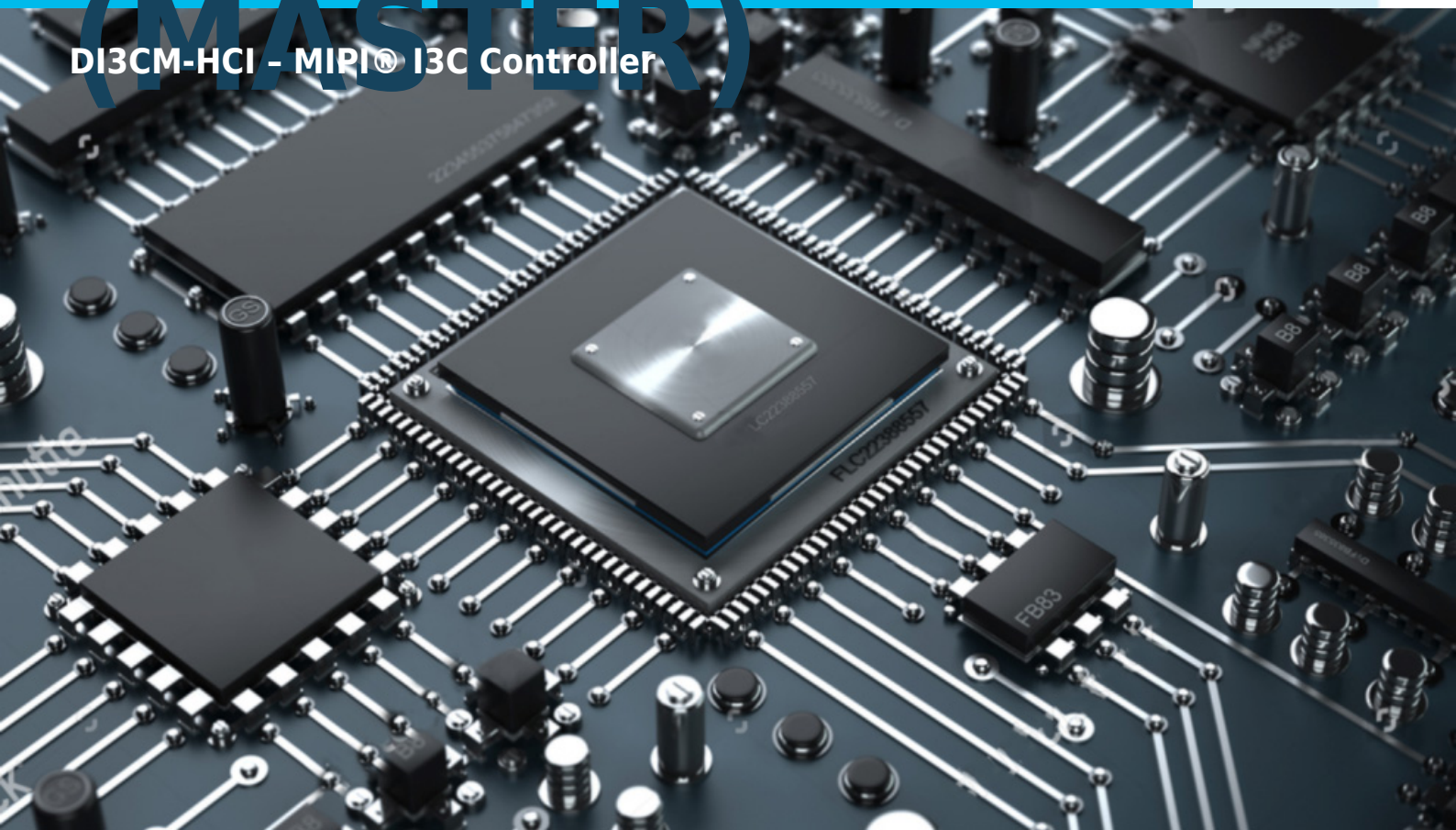

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI3CM-HCI – MIPI® I3C Contoller (Master)

for Smart Connectivity, Mobile, IoT, Automotive, and Next-Gen Embedded Systems

The **DI3CM-HCI** is a high-performance **MIPI® I3C Host Controller IP Core** engineered for design teams building faster, smarter, and more energy-efficient electronic systems. It acts as a modern connectivity backbone for **sensors, actuators, power-management units, and system controllers**, delivering a robust medium-speed control and utility interface that seamlessly links peripherals with the application processor.

Designed as a **future-proof replacement for legacy I²C and SPI**, the DI3CM-HCI offers:

- **Higher bandwidth** for data-intensive peripherals
- **Lower power consumption** for battery-sensitive designs
- **Reduced pin count and simplified board layout**
- **More reliable, feature-rich communication** suited for next-generation embedded architectures

With an integrated **Host Controller Interface (HCI)**, the DI3CM-HCI streamlines system integration, accelerates time-to-market, and enables scalable performance across **ASIC**, **SoC**, and **FPGA** platforms.

Optimized for Modern Electronic Design

Engineered for performance-driven applications, the DI3CM-HCI delivers:

- **Superior interoperability** with diverse smart peripherals
- **Efficient protocol management** and dynamic device enumeration
- **Easy scalability** for future system upgrades
- **Compact, low-power IP footprint** ideal for advanced designs

Whether you are developing consumer electronics, safety-critical automotive platforms, industrial IoT equipment, or ultra-compact wearable devices, the DI3CM-HCI provides the reliability and efficiency required for cutting-edge MIPI I3C communication.

Key Application Areas

Mobile & Consumer Electronics

- Camera modules
- Fingerprint and biometric sensors
- Haptic drivers and advanced UI components

IoT & Industrial Systems

- Environmental and multi-modal sensors
- Smart actuators and nodes
- Security modules and trusted elements

Automotive & Transportation

- ADAS sensor clusters
- Infotainment and smart-dashboard systems
- In-cabin monitoring and driver-awareness sensing

Wearables & Health Tech

- Motion tracking
- Health monitoring sensors
- Always-on, low-power embedded systems

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Technology-Agnostic IP Core

All DCD-SEMI IP Cores are fully technology-agnostic, ensuring **100% compatibility with any ASIC or FPGA vendor**, giving design engineers complete freedom in silicon platform selection and future migration.

Why Choose DI3CM-HCI?

The DI3CM-HCI represents DCD-SEMI's commitment to delivering **forward-looking, integration-friendly, and power-efficient connectivity IP**. Leveraging over two decades of engineering expertise, DCD-SEMI provides:

- Proven silicon-ready IP
- Extensive documentation and reference designs
- Direct access to expert technical support

With DI3CM-HCI, you can build **connected, intelligent, and future-ready devices** with confidence.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

KEY FEATURES

- Conforms to MIPI I3C Basic v1.1.1 Controller
- General compliance to MIPI I3C HCI Specification 1.1
- Up to 12.5 MHz clock frequency
- I3C SDR communication support
- I3C HDR-DDR communication support
- Legacy I2C communication support
- Dynamic address assignment (DAA) support
- In-Band Interrupts and Hot-Join support
- Common Command Codes (CCC) support
- Configurable size of memory buffers
- DMA handshake interface
- Power-efficient design with optional clock gating
- Configurable DAT/DCT size up to 16 slots
- Configurable FIFO size
- Generic memory-mapped interface with available wrappers:
  - AMBA – APB / AHB / AXI Bus
  - Altera Avalon Bus
  - Xilinx OPB Bus

APPLICATIONS

The I3C was initially intended for mobile applications as a single interface that can be used for any sensor. Modern smartphones that include a multitude of sensors and a slew of supporting logic lines are pushing the boundaries of both I²C and SPI. That's why I3C accommodates many sensors on the same communication bus, while eliminating additional logic signals needed to support interrupt or sleep mode functionality. Of course, The DI3CM-HCICore is useful for other applications than smartphones. It offers high speed data transfer at very low power levels, which is highly desirable for any embedded system. One of the examples are wearables (where multiple sensors are used in a very limited physical space and with stringent power restrictions). And if it's not enough it's worth to mention that DCD's IP Core as a standardized sensor interface can be utilized as a bus communication standard for touch sensing, always-on and low resolution cameras, acoustics, environmental sensors and transducers that currently use I²C, SPI, UART and others:

- Smartphones, tablets and laptops,
- IoT,
- Medical, health & fitness,
- Autonomous vehicles and ADAS,
- Embedded microprocessor boards,
- Low-power applications,
- Communication systems etc.

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices:

Device	LUTs	FFs	RAM
Xilinx xc7a200tsbv484-1 **SDR**	2477	893	1408bit
Xilinx xc7a200tsbv484-1 **HDR**	2820	908	1408bit
Xilinx xcvu19p_CIV-fsvb3824-1-e **SDR**	2273	741	1408bit
Xilinx xcvu19p_CIV-fsvb3824-1-e **HDR**	2649	758	1408bit

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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