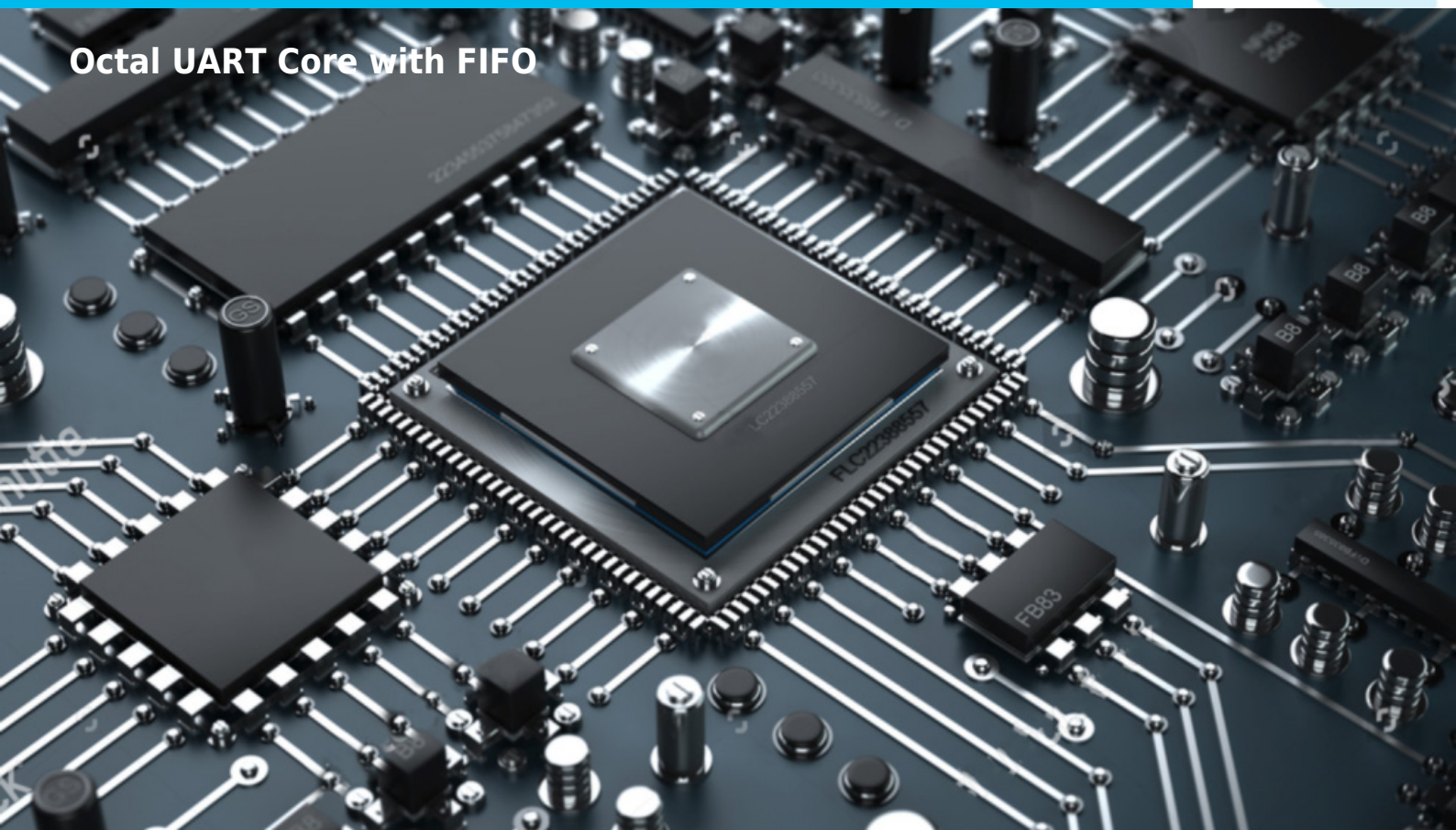
DIGITAL CORE DESIGN

D2698

Octal UART Core with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D2698 bridge to APB, AHB, AXI bus, it is an Octal UART Core **software compatible with the SC2698**. The core contains: **3 character receiver FIFO, extended baud rate, programmable receiver, and transmitter interrupts**. The D2698 Octal Universal Asynchronous Receiver/Transmitter (DUART) is a communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in polled or interrupt-driven systems and provides a modem interface. The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of 26 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter makes the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

- Software compatible with SCC2698 UART
- Configuration capability
- 8 full-duplex independent asynchronous receiver/transmitters
- 3 character FIFOs for each receiver channel
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 26 fixed rates: 50 to 115.2k baud
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode:
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- 2 Multi-function input and 2 I/O ports:
  - Can serve as clock, modem, or control inputs
  - Change of state detection on four inputs
- Multi-function output port:
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
  - FIFO states for DMA and modem interface
- Versatile interrupt system:
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watchdog timer for each receiver
- Maximum data transfer rates: 1X – 1Mb/sec, 16X – 1Mb/sec
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- Power down mode
- Receiver timeout mode
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

Data Bus Buffer – Provides an interface between external and internal data buses. It is controlled by the operation control block allowing read and write operations to take place between the controlling CPU and the DUART.
Operation Control – Receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus.
Interrupt Control – A single active-Low interrupt output (INTR) is provided which is activated upon occurrence of any of eight internal events. Associated with the interrupt system

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are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTR to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs MPO can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer. These pins may be used for DMA and modem control.

BRG – Baud Rate Generator – The baud rate generator operates from the oscillator or external clock input and is capable of generating 26 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates to 115.2kB. These will be in the 16X mode. All the baudrates are calculated for the external clock : 3.6864MHz. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

Counter-Timer – A programmable 16–bit divider that is used for generating miscellaneous clocks or generating timeout periods. These clocks may be used by any or all of the receivers and transmitters in the DUART or may be directed to an I/O pin for miscellaneous use.For Counter – Timer programming, please refer to the D2692's user manual.

Input Port – The inputs to this unlatched 8-bit port for each block can be read by the CPU, by performing a read operation as shown in Table 1. A High input results in a logic one, while a Low input results in a logic zero. The MPI pin can be programmed as an input to one of several Octal UART circuits. The function of the pin is selected by programming the appropriate control register. Change-of-state detectors are provided for MPI0 and MPI1 for each channel in each block. A High-to-Low or Low-to-High transition of the inputs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register. The input port pulse detection circuitry uses a global CLK signal for sampling, derived from one of the baud rate generator taps.

Multipurpose I/O Port – The multi-purpose pins (MPP) can be programmed as inputs or outputs using OPCR[7]. When programmed as inputs, the functions of the pins are selected by programming the appropriate control registers. When programmed as outputs, the two MPP1 pins (per block) will provide the transmitter ready (TxRDY) status for each channel and the MPP2 pins will provide the receiver ready or FIFO full (RxRDY/FFULL) status for each channel.

Multipurpose Output Port – This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see OPCR [2:0] and OPCR [6:4] – MPO Output Select).

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1. The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped. Each channel has 2 mode registers (MR1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software. Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

APPLICATIONS

- Serial Data communication applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA GX	4 252 / 1 860	304	150 MHz
ARIA V	4 088 / 1 892	304	174 MHz
CYCLONE2	5 896	304	148 MHz
CYCLONE3	5 972	304	180 MHz
CYCLONE4	5 968	304	166 MHz
CYCLONE5	4 088 / 1 860	304	170 MHz
STRATIX2	4 228 / 1 860	304	212 MHz
STRATIX3	4 124 / 1 976	304	331 MHz
STRATIX4	4 104 / 2 108	304	337 MHz
STRATIX5	4 224 / 1 960	304	339 MHz
STRATIX2 GX	4 228 / 1 860	304	218 MHz
MAX10	5 824	304	170 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment

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    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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