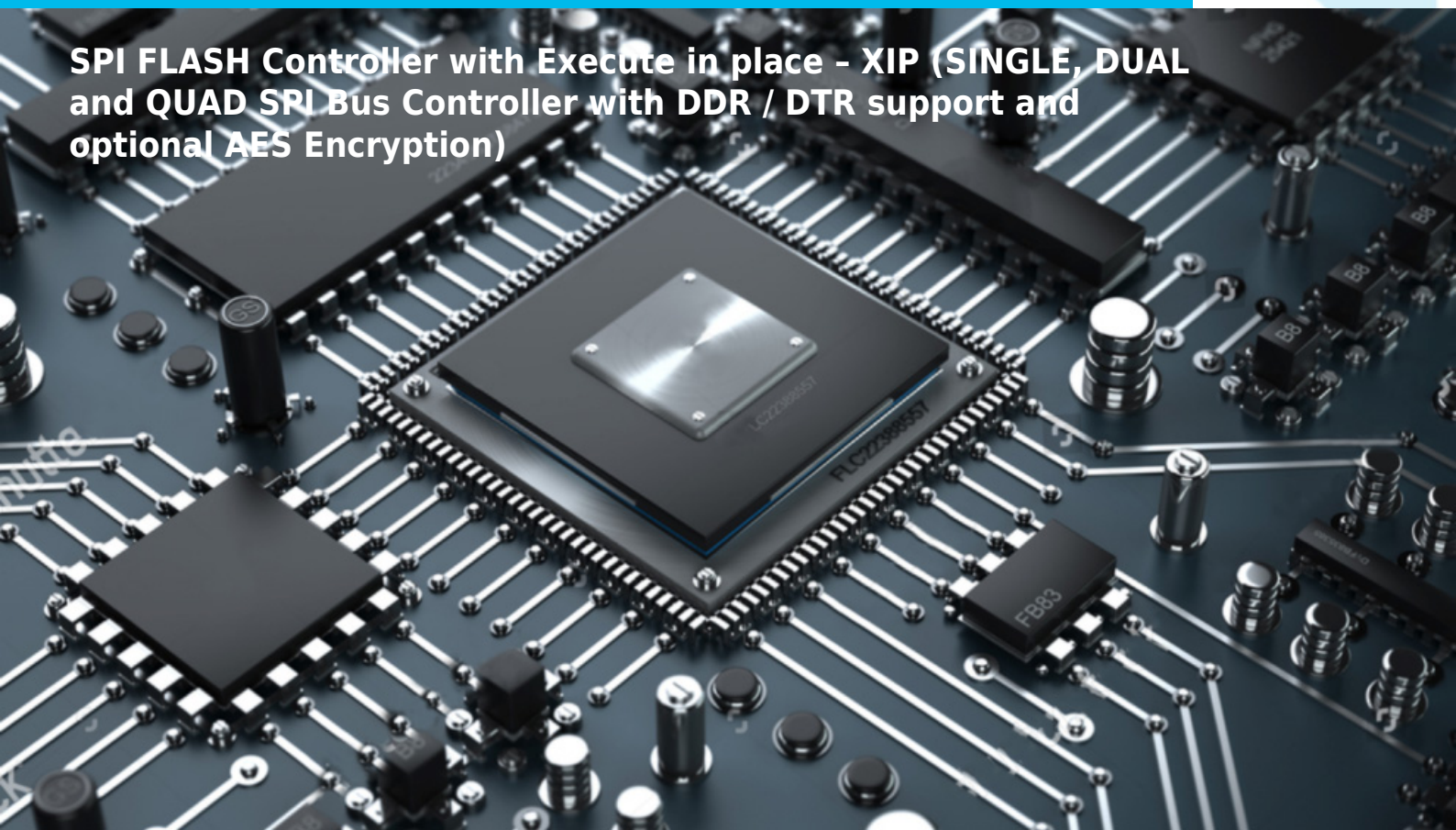
DIGITAL CORE DESIGN

DFSPI

SPI FLASH Controller with Execute in place – XIP (SINGLE, DUAL and QUAD SPI Bus Controller with DDR / DTR support and optional AES Encryption)



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DFSPI bridge to APB, AHB, AXI bus, it is a fully configurable **SINGLE, DUAL, QUAD, and OCTAL** SPI master/slave device, which allows the user to configure polarity and phase of the serial clock signal SCK. As an option, the DFSPI controller has built-in support for **HyperBus™** specification and **xSPI** (Expanded Serial Peripheral Interface – JESD251A) specification. The SPI Controller allows easy communication with the most available SPI FLASH memories. **The DFSPI fully supports NOR & NAND Flash Memory**.

A serial clock line (SCK) synchronizes the shifting and sampling of the information on the serial data lines. It is a technology-independent design that can be implemented in various process technologies. The DFSPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate the most available synchronous serial peripheral devices.

The DFSPI can automatically drive selected by SSCR (Slave Select Control Register) slave select outputs (SS3O – SS0O), and address SPI slave device to exchange serially shifted data. It supports two DMA modes: single transfer and multi-transfer. These modes allow DFSPI to interface with higher-performance DMA units, which can interleave their transfers between CPU cycles or execute multiple byte transfers. DFSPI is **fully customizable**, delivering it in the exact configuration that meets users' requirements.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- NOR & NAND Flash Memory Support
- Set of software-accessible control registers to execute any Flash memory command
- Supports any device clock frequency, polarity, and phase,
- Programmable baud rate generator,
- Built-in FLASH Commands decoder supports most popular FLASH devices,
- Optional built-in AES Encoder/Decoder
- DMA support
- Optional support for various SPI Bus Standards: HyperBus™, xSPI
- Compliant with AMBA2 Specification, support APB, AHB, AXI bus interfaces
- Single, Dual, Quad, and OCTAL SPI transfer/reception
- Execute in place – XIP functionality support
- Data Bus Size configuration to 8, 16, or 32 bits wide
- Optional FIFO size extension
- Maximum supported Flash address range – 32 bits
- Up to 4 SPI slaves can be addressed
  - Software Slave Select Output – SSO – selection
  - Automatic Slave Select outputs assertion
- System error detection
- Interrupt generation
- Bit rates generated as 1/ 2.. 1/255 of the system clock.
- Four SPI transfer formats supported: CPOL/CPHA.
- Simple interface allows easy connection to microcontrollers
- Fully synthesizable, static synchronous design with no internal tri-states

UNIT SUMMARY

Shift Register – The heart of the DFSPI controller. It shifts in and out data from the DFSPI controller regarding to the appropriate edge of the SCK.
Receiver FIFO – The Rx FIFO by default is 256 Bytes deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if interrupt is enabled, the DFSPI will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full and will not accept any next byte. Once the RX FIFOO is full, internal logic stops SPI operations to prevent FIFO overflow.
Transmitter FIFO – The DFSPI transmits data through DQ lines as soon as the CPU loads data into the Tx FIFO. When the TX FIFO is full, DFSPI prevents any further loads into it. When the next TX FIFO load occur, data is not written and the TX OVERFLOW error flag is set. Loading next data to the Tx FIFO will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.
Baudrate Generator – Used to generate the master SCK Clock in selected rate. System allows flexible SCK rate definition in range of CLK / 2 up to CLK/256, depending on the value written to the BauRate Register.
SPI Clock Logic – This module controls phase and polarity of generated/received SCK signal. On correct SCK edge generates shift signal to SPI Shift register.
System Bus Wrapper – Allows connection of the DFSPI CPU

interface to peripheral Bus of the SoC system.
FLASH Commands decoder – The decoder recognizes the command code and set the transfer/reception parameters accordingly. Decoder supports most commands of the major FLASH types. For specific commands or memories user can switch the decoder off, then all the parameters need to be set manually. With decoder disabled, the DFSPI can support any FLASH and all the possible commands types.
AES Encoder / Decoder – This is an optional module, added as special request. The AES module allows the FLASH data to be encrypted with selected AES 128 or AES 256 encryption standards. With the AES module, all encryption operations are done fully automatic and do not require special effort during programming and XIP operations. The AES module is intended for applications with high code security demand. AES require the data buffer with the size of 64 bytes. With AES module all FLASH read/write operations require more time needed for the encryption process.

XIP – EXECUTE IN PLACE MODE

In the XIP mode, the DFSPI allows direct Read or Write of data from SPI FLASH memories. In this mode the DFSPI operates as a serial-to-parallel converter between SPI flash and CPU. To operate in the XIP mode, the SPI Flash needs to be configured first. Once it is correctly configured, XIP operation with DFSPI is ready just after power-up, without any further software effort. Default setting of the DFSPI Controller allows FLASH read using the preset READ Command just after power up. Other, specific commands or memory settings, require to be set in software first, or defined as default values before the DFSPI Controller synthesis. After memory configuration the memory space can be easily read through the DFSPI. For communication optimization, the DFSPI allows easy protocol configuration using XIP Control registers bits, allowing XIP operation without any software overhead.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

PERFORMANCE

To provide you with the most accurate and detailed insights about the Lattice performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVEVERABLES

- **Source code:**
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - EDIF Netlist
- **VHDL or VERILOG test bench environment**
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- **Technical documentation**
  - Installation notes
  - HDL core specification
  - Datasheet
- **Linux Driver – Optional**
- **Synthesis scripts**
- **Example application**
- **Technical support**
  - IP Core implementation support
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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