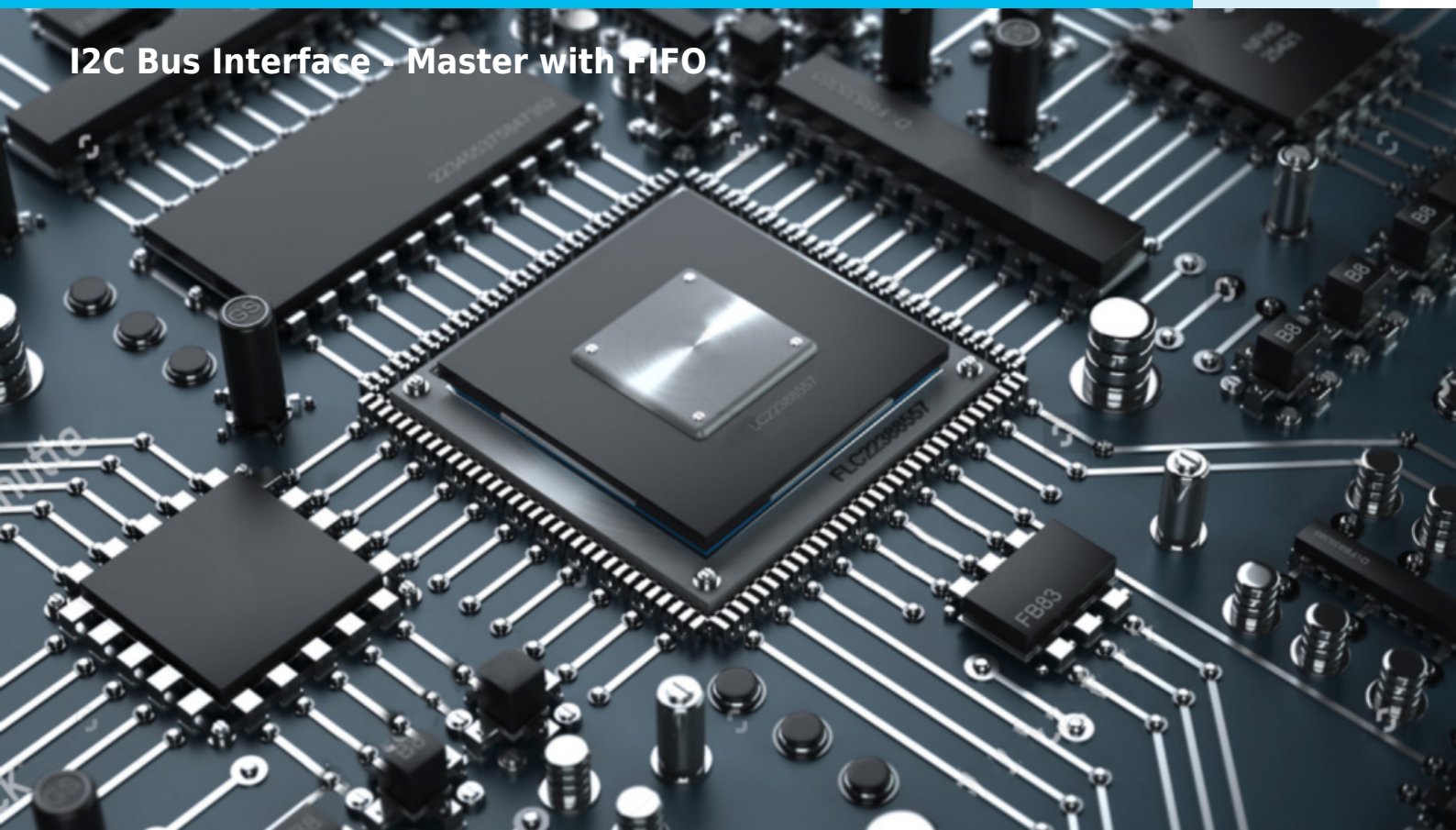
DIGITAL CORE DESIGN

DI2CM-FIFO

I2C Bus Interface - Master with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CM-FIFO bridge to APB, AHB, AXI bus, this core provides an interface between a microprocessor/microcontroller and I2C bus. It can work as:

- a master transmitter or
- master receiver

depending on a working mode determined by the microprocessor/microcontroller. The DI2CM-FIFO core **incorporates all features required by the latest I2C specification**, including clock synchronization, arbitration, multi-master systems, and high-speed transmission mode. The built-in **timer allows operation from a wide range of clk frequencies**. The DI2CM-FIFO is a **technology-independent design** that can be implemented in a variety of process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Conforms to v.6.0 of the I2C specification
- Master operation
  - Master transmitter
  - Master receiver
- Support for all transmission speeds
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - **Fast Plus (up to 1 Mb/s)**
  - **High Speed (up to 3,4 Mb/s)**
  - **ULTRA-FAST (up to 5 Mb/s)**
  - **Configurable FIFO size up to 256 Bytes**
  - **Configurable SDA/SCL glitch filter**
  - **Software programmable SDA/SCL bus timings**
- Arbitration and clock synchronization
- Support for multi-master systems
- Support for both 7-bit and 10-bit addressing formats on the I2C bus
- Interrupt generation
- Allows operation from a wide range of input clock frequencies (build-in 12-bit clock timer)
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

CPU Interface – Performs the interface functions between DI2CM-FIFO internal blocks and microprocessor. Allows easy connection between the core and a microprocessor / microcontroller system including: APB, AHB, 8051, 80251, others. Includes FIFO management.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.
Control Register – Contains five control bits, used for performing all types of I^2C Bus transmissions.
Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CM-FIFO core.
Clock Generator – Performs generation of the serial clock.
Input Filter – Performs spike filtering.
Clock Synchronization – Performs clock synchronization.
Arbitration Logic – Performs arbitration during operations in multi-master systems.
Timer – Allows operation from a wide range of the input frequencies. It is programmed by the user before transmission and can be reprogrammed to change the SCL frequency.

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Technology	Optimization	Gates	F_{max}
0.18 typical	area	3 300	100 MHz

0.18 typical	speed	3 600	300 MHz
0.11 typical	area	3 200	100 MHz
0.11 typical	speed	3 400	400 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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