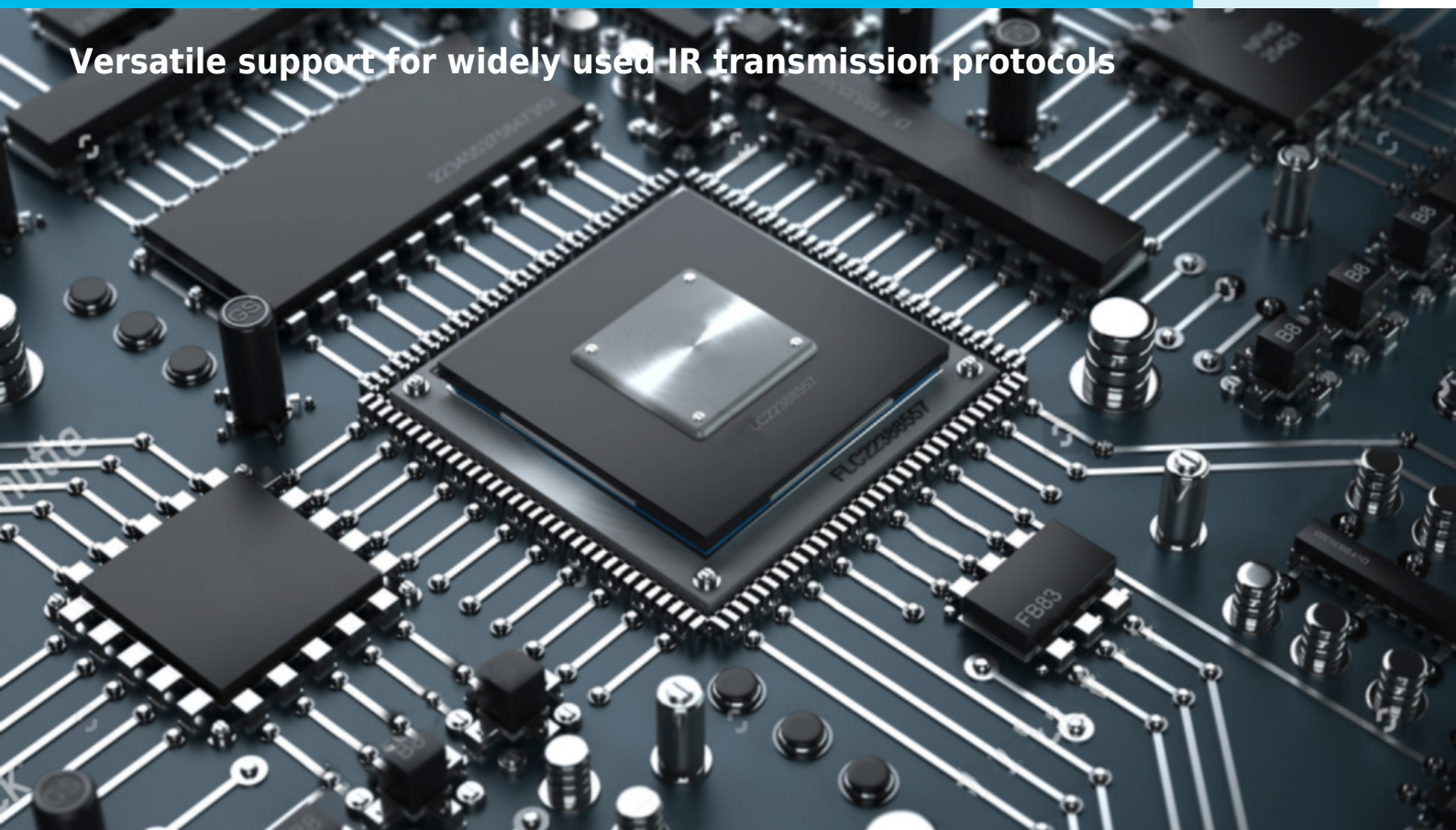
DIGITAL CORE DESIGN

DIRDA

Versatile support for widely used IR transmission protocols



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

Our efficient Core performs serial to parallel conversion on data received from an IR Receiver Diode. The processor can read the complete status of the DIRDA at any time during the functional operation. The DIRDA includes a programmable internal Prescaler which is able to divide a timing reference clock input by divisors of 1 to 128 and produce a clock for driving internal receiver logic. We also equipped our core with a processor interrupt system. Interrupts can be programmed according to your requirements, minimizing the computing required to handle the communications link. It can be provided with the small 8bit SRAM-like interface and APB slave interface. In MODE0 DIRDA decode the whole IR frame, and detect transmission errors and key release. In MODE1, internal FIFO is activated allowing 32 symbols to be stored during signal receive. Interrupt trigger level register may set any value from 1 to 32 symbols. All gathered makes it an ideal choice for prevalent IR protocols implementations like NEC, SIRC, TC9012 data format, or other non-standard IR protocols.

DESIGN FEATURES:

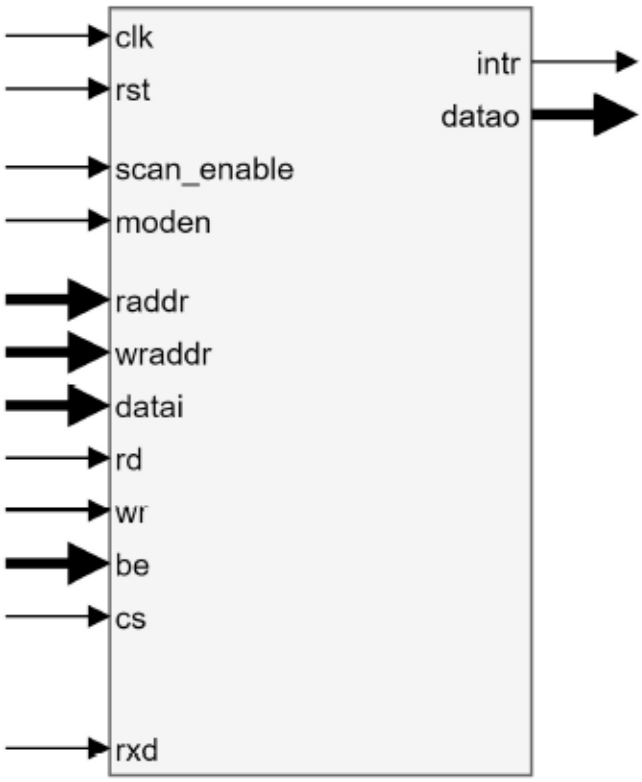
ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Enabling and disabling controller via register
- Two working modes:
  - MODE0 - standard IR protocols decoding
  - MODE1 - symbols width detection for any standard or non-standard IR data format
- Support for any configuration of the following protocols (MODE0):
  - NEC with Simple Repeat Code
  - NEC with Full Repeat Code
  - TC9012 data format
  - SIRC (SONY)
- Support for masked and not masked interrupts:
  - Symbol overflow interrupt (MODE1)
  - Symbol timeout interrupt (MODE1)
  - Symbol received interrupt (MODE1)
  - Key release interrupt (MODE0)
  - Data overflow interrupt (MODE0)
  - Data frame format error interrupt (MODE0)
  - Data received interrupt (MODE0)
- Interrupts flags clearance via write to register
- Configurable reset
- Configurable data bus width
- Reference clock frequency in range of 1MHz-128MHz

BLOCK DIAGRAM



DELIVERABLES

The list of deliverables consists of:

- Source Code
  - VERILOG Source code
- VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet

- Synthesis scripts
- Technical support
  - IP Core implementation support
  - 12 months of maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited.

There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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