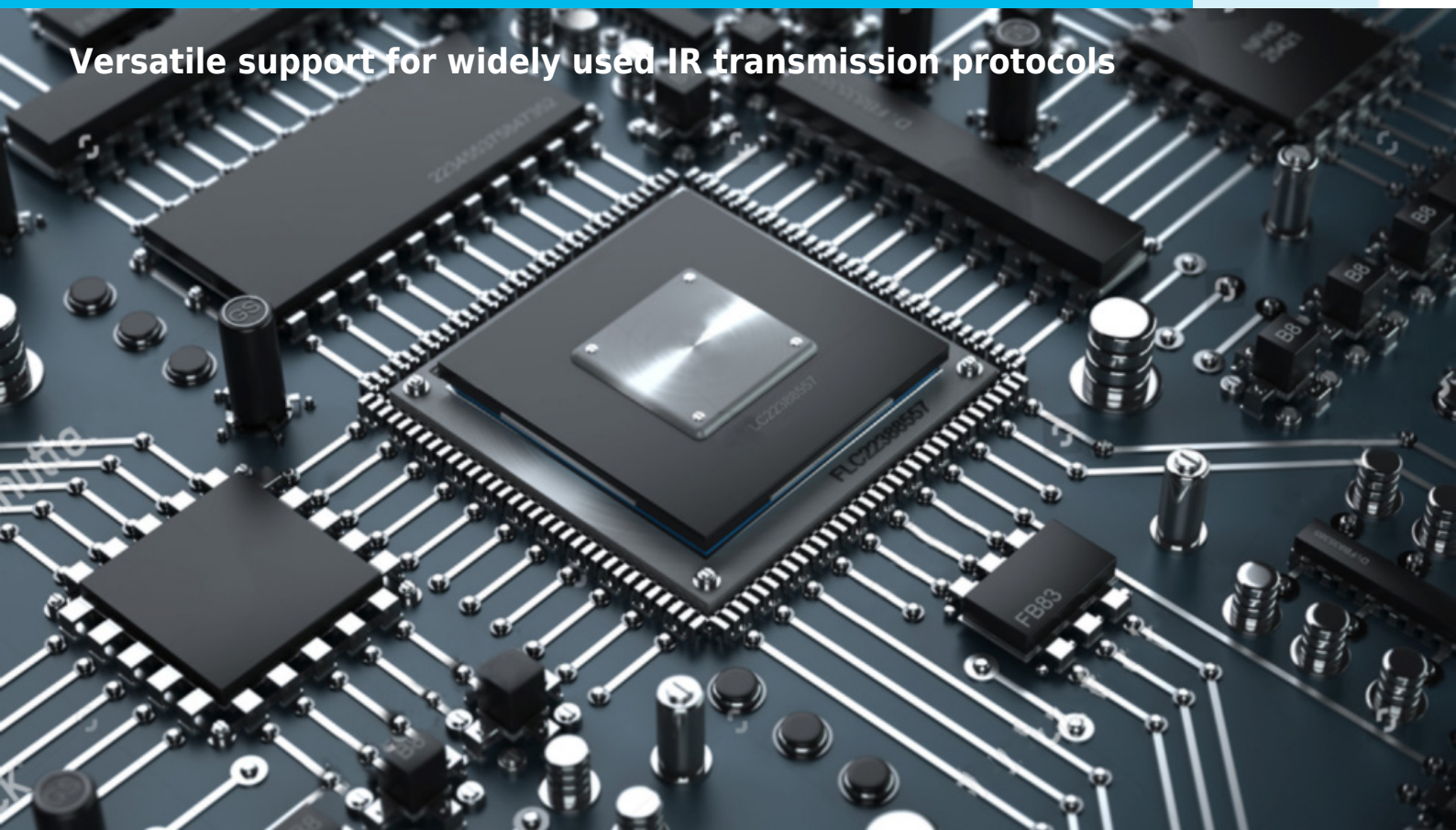
DIGITAL CORE DESIGN

DIRDA

Versatile support for widely used IR transmission protocols



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DIRDA IP Core – Infrared Receiver Decoder for FPGA & ASIC Designs

The **DIRDA IP Core** from **DCD-SEMI** is a compact and efficient **infrared (IR) receiver controller** designed to perform **serial-to-parallel conversion** of data received from an **IR receiver diode**. Optimized for **FPGA and ASIC implementations**, DIRDA enables reliable decoding of popular and custom **IR remote-control protocols** while significantly reducing processor workload.

The core allows the processor to **read full status information at any time** during operation, ensuring deterministic control and easy system integration.

Flexible Timing and Low CPU Overhead

DIRDA integrates a **programmable internal prescaler** that divides the reference timing clock by values from **1 to 128**, generating an optimized internal clock for the receiver logic. This flexibility allows accurate decoding across a wide range of IR carrier frequencies and protocols.

To further minimize CPU involvement, the core features a **fully programmable interrupt system**. Interrupts can be configured to match application-specific requirements, reducing polling overhead and improving overall system efficiency.

Dual Operating Modes for Maximum Versatility

The DIRDA IP Core supports two distinct operating modes:

MODE0 – Full Frame Decoding

- Decodes the **entire IR frame in hardware**
- Detects **transmission errors**
- Identifies **key release events**

MODE1 – FIFO-Based Symbol Capture

- Activates an internal **FIFO buffer**
- Stores up to **32 received symbols**
- **Programmable interrupt trigger level** (1–32 symbols)

This dual-mode architecture enables both **fully autonomous decoding** and **raw symbol processing**, depending on system requirements.

Interface Options and SoC Integration

DIRDA can be delivered with:

- **Small 8-bit SRAM-like interface** for minimal systems
- **AMBA APB slave interface** for modern SoC designs

The core is fully compatible with **technology-independent FPGA and ASIC flows**.

Supported and Target IR Protocols

DIRDA is an ideal solution for implementing widely used IR protocols, including:

- **NEC**
- **SIRC (Sony IR)**
- **TC9012**
- Custom and non-standard IR protocols

Typical Applications

- IR remote control receivers
- Consumer electronics (TVs, set-top boxes, audio devices)
- Industrial control panels
- FPGA-based embedded systems
- ASIC designs requiring low-power IR decoding

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.

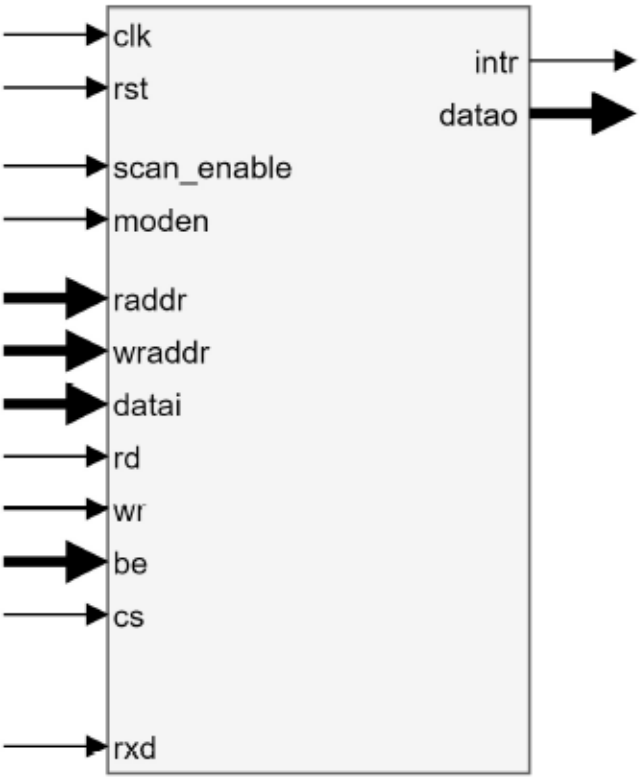
ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Enabling and disabling controller via register
- Two working modes:
  - MODE0 - standard IR protocols decoding
  - MODE1 - symbols width detection for any standard or non-standard IR data format
- Support for any configuration of the following protocols (MODE0):
  - NEC with Simple Repeat Code
  - NEC with Full Repeat Code
  - TC9012 data format
  - SIRC (SONY)
- Support for masked and not masked interrupts:
  - Symbol overflow interrupt (MODE1)
  - Symbol timeout interrupt (MODE1)
  - Symbol received interrupt (MODE1)
  - Key release interrupt (MODE0)
  - Data overflow interrupt (MODE0)
  - Data frame format error interrupt (MODE0)
  - Data received interrupt (MODE0)
- Interrupts flags clearance via write to register
- Configurable reset
- Configurable data bus width
- Reference clock frequency in range of 1MHz-128MHz

BLOCK DIAGRAM



PERFORMANCE

For precise AMD performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.