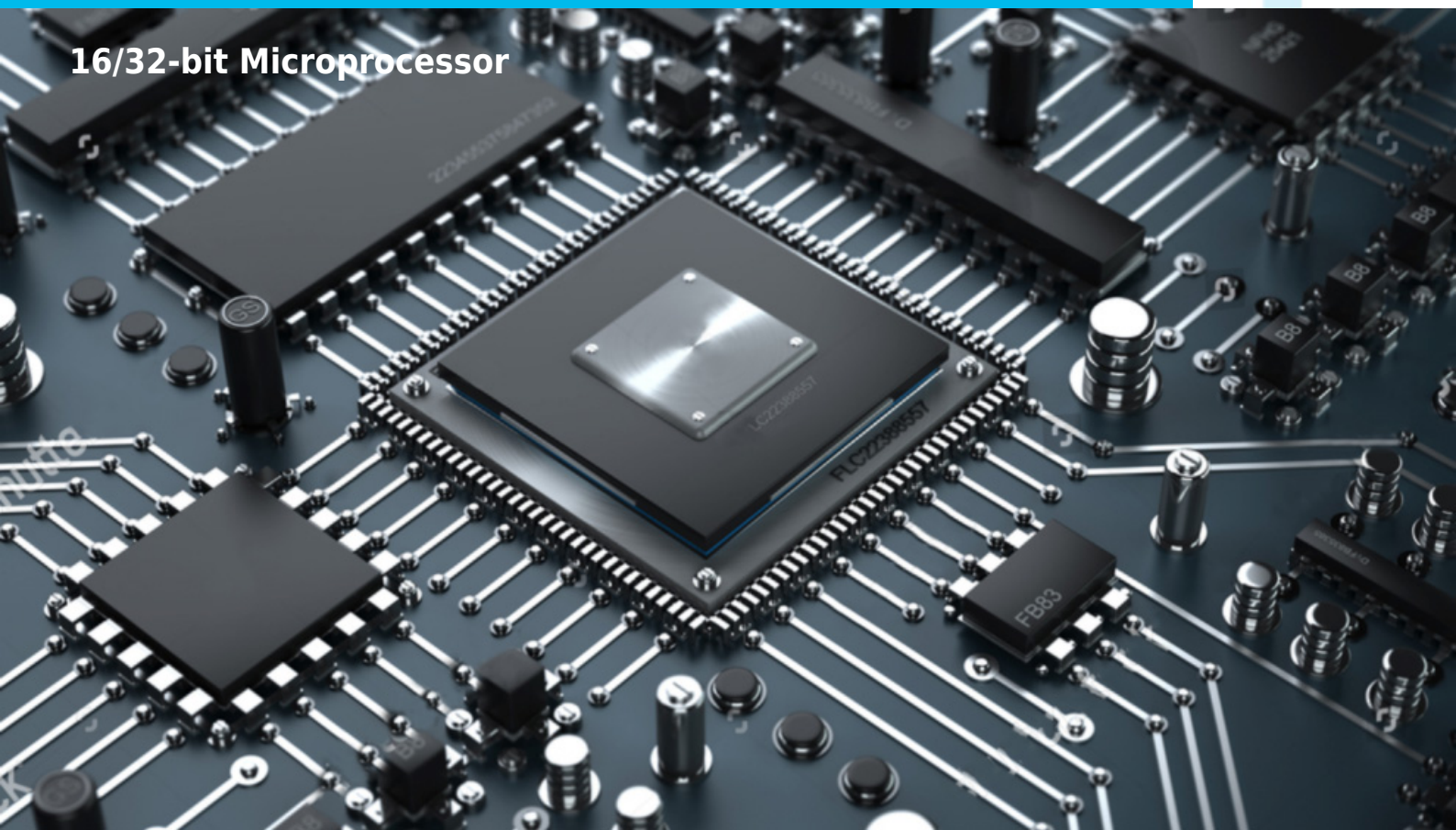
DIGITAL CORE DESIGN

D68000-CPU32

16/32-bit Microprocessor



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D68000-CPU32 Soft Processor IP Core

The **D68000-CPU32** is a high-performance, **32-bit soft CPU IP core** that is fully **binary-compatible with the industry-standard Motorola 68000 CPU32 architecture** (MC68020 CPU32 variant). Designed for seamless reuse of legacy software, the core ensures full **code compatibility with existing 68000/CPU32 toolchains and applications**, making it ideal for industrial, automotive, and embedded SoC designs.

The D68000-CPU32 features a **16-bit data bus** and a **24-bit address bus**, delivering an optimal balance between performance and silicon efficiency. Its **enhanced instruction set** improves execution efficiency and throughput compared to the classic 68000 core, enabling faster program execution without software modification.

For efficient development and debugging, the core integrates a **built-in DoCD-BDM debug interface**, allowing real-time inspection, control, and system bring-up. The IP is delivered as a **fully verified soft core**, complete with an **automated testbench and comprehensive regression test suite**, supporting straightforward validation and integration at every stage of the **SoC design and verification flow**.

The **D68000-CPU32 IP core** is a proven solution for engineers seeking a **68000-compatible processor IP** with improved performance, robust debug capabilities, and production-ready verification collateral.

DCD-SEMI D68000 FAMILY – IP CORE COMPARISON TABLE

Feature / IP Core	D68000	D68000-CPU32	D68000-CPU32+
Architecture Compatibility	Motorola 68000	Motorola CPU32	Motorola CPU32+ (MC68020-class)
Binary Compatibility	68000 software	CPU32 software	CPU32+ software
Data Bus Width	16-bit	32-bit	32-bit
Address Bus Width	24-bit	32-bit	32-bit
Instruction Set	Classic 68000	Extended CPU32	Enhanced CPU32+
Execution Performance	Baseline 68000	Higher than 68000	Highest in D68000 family
Target Use Case	Pure 68000 legacy replacement	CPU32 MCU migration	High-performance CPU32+ systems
Debugger Interface	DoCD-BDM (optional)	DoCD-BDM	**Built-in DoCD-BDM**
Software Recompilation Required	□ No	□ No	□ No
FPGA / ASIC Ready	□ Yes	□ Yes	□ Yes
Technology Independent	□ Yes	□ Yes	□ Yes
Automated Testbench	□ Yes	□ Yes	□ Yes
Verification Test Suite	Complete	Complete	Complete
Typical Applications	Industrial legacy control	Automotive / industrial MCU	Automotive ECUs, long-lifecycle SoCs
Best For	Lowest-risk 68000 drop-in	Balanced performance & compatibility	Maximum performance with CPU32+ ISA

HOW TO CHOOSE

- **Choose D68000** if you need a **pure 68000 replacement** with minimal bus width and maximum legacy fidelity.
- **Choose D68000-CPU32** if your software targets **CPU32 MCUs** and needs higher performance with a 32-bit bus.
- **Choose D68000-CPU32+** if you want **the fastest 68k-compatible core**, extended instruction set, and built-in debug for modern FPGA/ASIC designs.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Software compatible with industry standard 68000's **CPU32**
- DoCD-BDM on-chip debugger as in CPU32
- VBR register
- Optimized shifts and rotations
- Idle cycles removed to improve performance
- Shorter effective address calculation time
- Bus cycle timings identical to 68000
- 32-bit data and address registers

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.

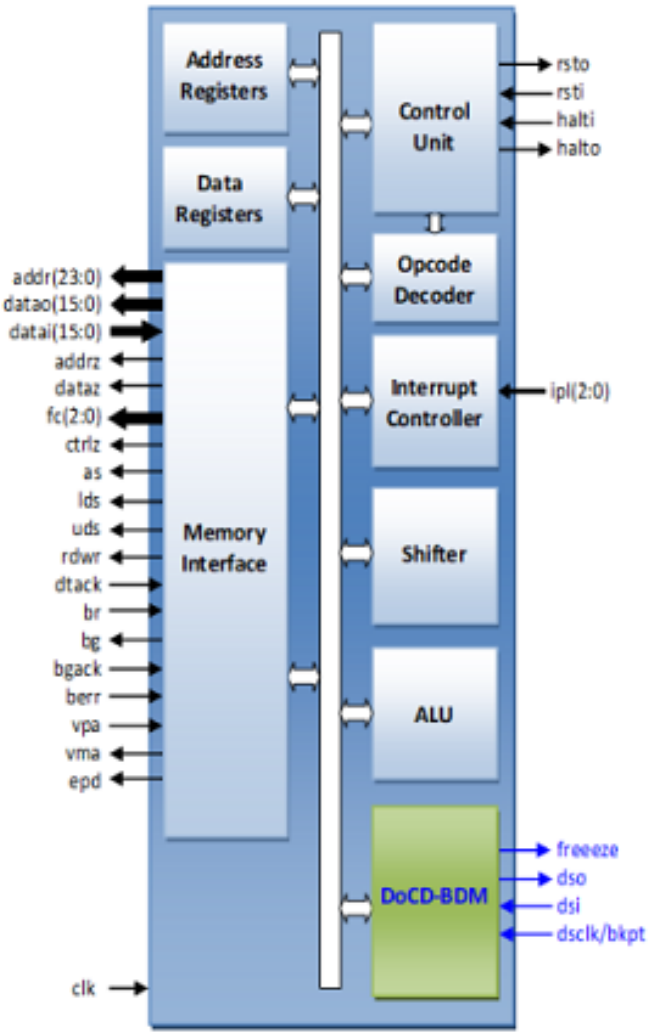
- 16 addressing modes:
  - Direct:
    - Data register direct – Dn
    - Address register direct – An
  - Indirect:
    - Register indirect – (An)
    - Post-increment register indirect – (An+)
    - Pre-decrement register indirect – (-An)
    - Register indirect with offset – (d16,An)
    - Indexed register indir. with offset – (d8,An,Xn)
    - Indexed register indir. with offset and base displacement – (bd,An,Xn)
  - PC relative:
    - with offset(d16,PC); with index and offset – (d8,PC,Xn)
    - with index offset and base displacement – (bd,PC,Xn)
  - Absolute data:
    - Absolute short (.W)
    - Absolute long (.L)
  - Immediate data:
    - Immediate – #data
    - Quick immediate – #n
  - Implied
- 5 data types supported:
  - bits, BCD
  - bytes, words and long words
- Arithmetic Logic Unit includes:
  - 8,16,32-bit arithmetic & logical operations
  - 16×16, 32×32 bit signed and unsigned multiplication
  - 32/16, 32/32, 64/32 bit signed and unsigned division
  - Boolean operations
- Interrupt controller:
  - 7 priority levels interrupt controller
  - Unlimited number of virtual interrupt sources
  - Vectored and auto-vectored modes
  - Format $0, $2, $C exceptions support as in CPU32
- Memory interface includes:
  - Up to 16 MB of address space
  - 16-bit data bus
  - Asynchronous bus control
- M6800 family synchronous interface
- 3- and 2- wire bus arbitration
- Supervisor and user modes
- Fully synthesizable, static synchronous design with no internal tri-states

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator and related logic, such as arithmetic unit, logic unit, multiplier and divider. BCD operation are executed in this unit and condition code flags (N-negative, Z-zero, C-carry V-overflow) for most instructions.
Shifter – Performs shifting operations for the appropriate instructions, mainly for rotation, shift and bit operations.
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. Contains SR (status register is consisted of two portions: supervisor byte and user byte) and its related logic.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all blocks.
Memory Interface – Contains memory access related registers. It performs the memory addressing instructions code fetching and data transfers. It is responsible for all external bus cycle actions, such as: read & write, repeated read & write, halt and resume of bus cycles, bus arbitration provided by 3- and 2- wire system, correct bus and address errors handling, wait states cycle insertion and M6800 synchronous cycle generation.
Interrupt Controller – Interrupt Control module is responsible for the interrupt manage system for the external & internal interrupts and exceptions processing. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.
Address registers – Contains 32-bit A0 to A6 address registers, two stack pointers USP (user SP) and SSP (Supervisor SP), 32-bit Program counter and related logic to perform word and long address operations. Effective address operations are executed in this unit.
Data registers – Contains 32-bit data registers D0 to D7 and related logic to perform byte, word and long data operations.
DoCD-BDM – it's a hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, BDM provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, patch user code, read/write any contents of microprocessor including all registers, memories and user connected peripherals. Hardware breakpoints can be set and controlled on program and data memories. One additional pin FREEZE indicates the state of the CPU. It is active, when CPU is halted and debugger is in action. The BDM system includes **SPI-like serial interface** and complete set of tools, to communicate and work with core in a real time debugging.

BLOCK DIAGRAM

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.



PERFORMANCE

The following tables give a survey about the Core area and performance in ASIC devices after Place & Route (all CPU features and peripherals included):

Device	Gates
0.18u typical	29 000

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.