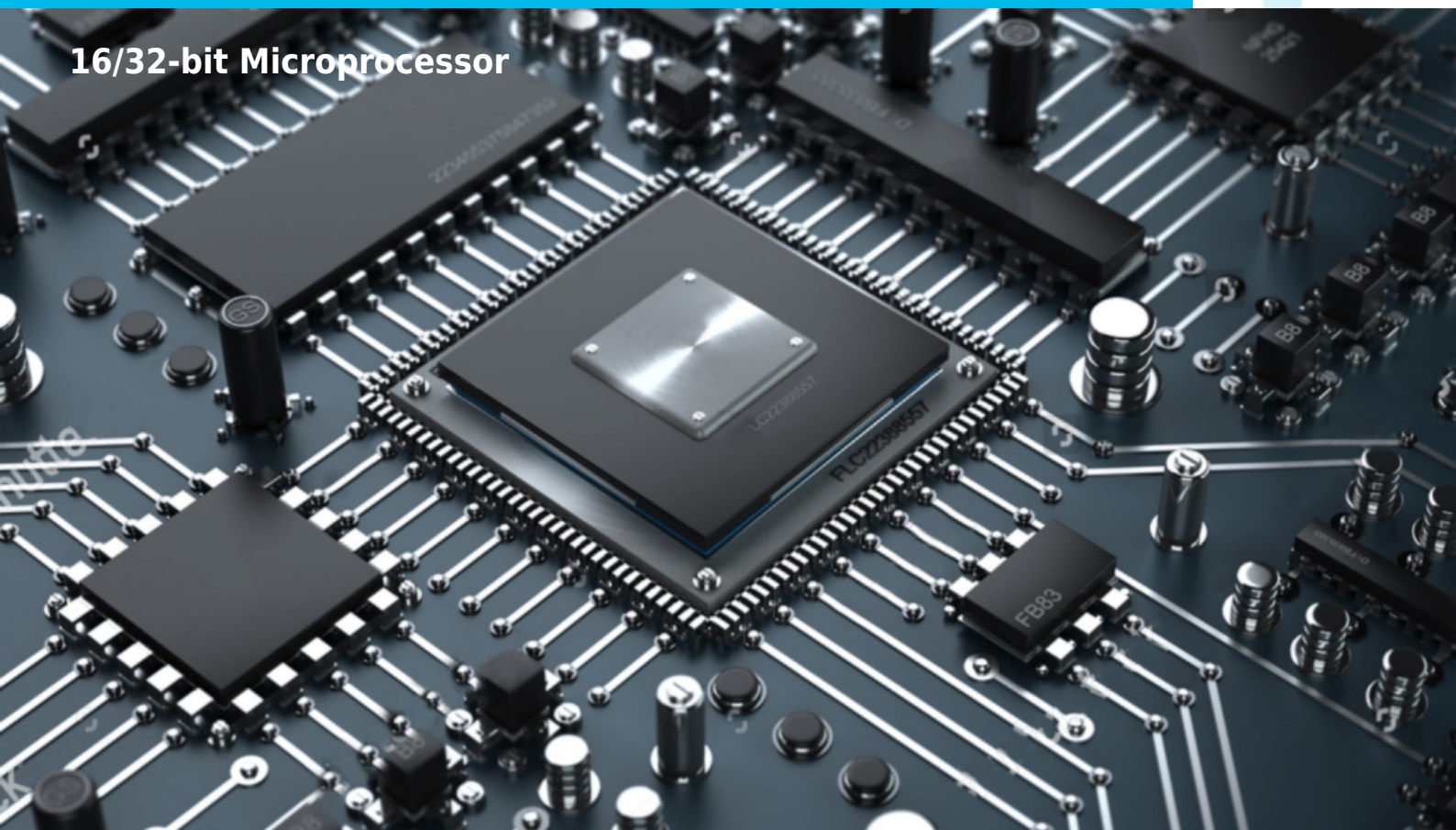
DIGITAL CORE DESIGN

D68000-CPU32

16/32-bit Microprocessor



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D68000-CPU32 soft core is binary-compatible with the industry standard 68000's CPU32 version of the 32-bit microcontroller. The D68000-CPU32 has a 16-bit data bus and a 24-bit address data bus. It is code compatible with the 68000's **CPU32 (version of MC68020)**. The D68000-CPU32 has an improved instruction set, which allows program execution with higher performance than the standard 68000 core. It contains a built-in **DoCD-BDM debugger** interface. The D68000-CPU32 is delivered with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Software compatible with industry standard 68000's **CPU32**
- DoCD-BDM on-chip debugger as in CPU32
- VBR register
- Optimized shifts and rotations
- Idle cycles removed to improve performance
- Shorter effective address calculation time
- Bus cycle timings identical to 68000
- 32-bit data and address registers
- 16 addressing modes:
  - Direct:
    - Data register direct – Dn
    - Address register direct – An
  - Indirect:
    - Register indirect – (An)
    - Post-increment register indirect – (An+)
    - Pre-decrement register indirect – (-An)
    - Register indirect with offset – (d16,An)
    - Indexed register indir. with offset – (d8,An,Xn)
    - Indexed register indir. with offset and base displacement – (bd,An,Xn)
  - PC relative:
    - with offset(d16,PC); with index and offset – (d8,PC,Xn)
    - with index offset and base displacement – (bd,PC,Xn)
  - Absolute data:
    - Absolute short (.W)
    - Absolute long (.L)
  - Immediate data:
    - Immediate – #data
    - Quick immediate – #n
  - Implied
- 5 data types supported:
  - bits, BCD
  - bytes, words and long words
- Arithmetic Logic Unit includes:
  - 8,16,32-bit arithmetic & logical operations
  - 16×16, 32×32 bit signed and unsigned multiplication
  - 32/16, 32/32, 64/32 bit signed and unsigned division
  - Boolean operations
- Interrupt controller:
  - 7 priority levels interrupt controller
  - Unlimited number of virtual interrupt sources
  - Vectored and auto-vectored modes
  - Format $0, $2, $C exceptions support as in CPU32
- Memory interface includes:
  - Up to 16 MB of address space
  - 16-bit data bus
  - Asynchronous bus control
- M6800 family synchronous interface
- 3- and 2- wire bus arbitration
- Supervisor and user modes
- Fully synthesizable, static synchronous design with no internal tri-states

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator and related logic, such as arithmetic unit, logic unit, multiplier and divider. BCD operation are executed in this unit and condition code flags (N-negative, Z-zero, C-carry V-overflow) for most instructions.
Shifter – Performs shifting operations for the appropriate instructions, mainly for rotation, shift and bit operations.
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. Contains SR (status register is consisted of two portions: supervisor byte and user byte) and its related logic.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all blocks.
Memory Interface – Contains memory access related registers. It performs the memory addressing instructions code fetching and data transfers. It is responsible for all

external bus cycle actions, such as: read & write, repeated read & write, halt and resume of bus cycles, bus arbitration provided by 3- and 2- wire system, correct bus and address errors handling, wait states cycle insertion and M6800 synchronous cycle generation.

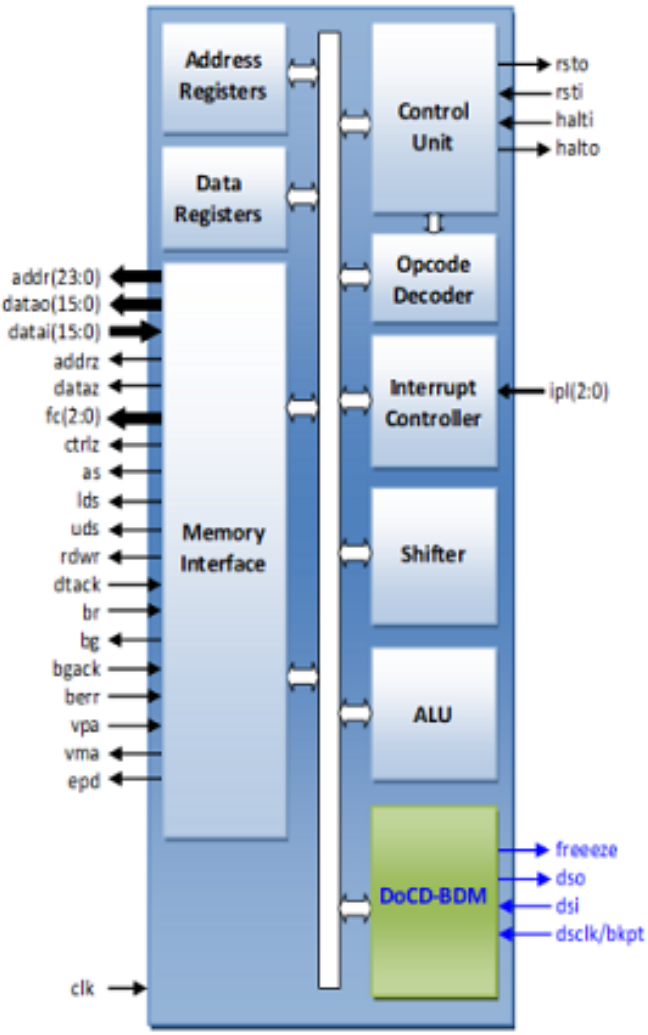
Interrupt Controller – Interrupt Control module is responsible for the interrupt manage system for the external & internal interrupts and exceptions processing. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.

Address registers – Contains 32-bit A0 to A6 address registers, two stack pointers USP (user SP) and SSP (Supervisor SP), 32-bit Program counter and related logic to perform word and long address operations. Effective address operations are executed in this unit.

Data registers – Contains 32-bit data registers D0 to D7 and related logic to perform byte, word and long data operations.

DoCD-BDM – it's a hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, BDM provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, patch user code, read/write any contents of microprocessor including all registers, memories and user connected peripherals. Hardware breakpoints can be set and controlled on program and data memories. One additional pin FREEZE indicates the state of the CPU. It is active, when CPU is halted and debugger is in action. The BDM system includes **SPI-like serial interface** and complete set of tools, to communicate and work with core in a real time debugging.

BLOCK DIAGRAM



PERFORMANCE

To provide you with the most accurate and detailed insights about the Intel performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVERABLES

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - VCS automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support

- IP Core implementation
- 12 months maintenance
  - Delivery of the IP Core and documentation updates
  - Phone & email support
  - Design consulting

PINS DESCRIPTION

PIN	TYPE	Active	DESCRIPTION
clk	input	high	Global clock
scan_enable	input	high	Scan enable. Should be '0' for normal work.
rsti	input	low	Global reset input
halti	input	low	Halt input
vpa	input	low	Valid peripheral address
ipl[2:0]	input	low	Interrupt control
dtack	input	low	Data transfer acknowledge
br	input	low	Bus request
bgack	input	low	Bus grant acknowledge
datai[15:0]	input	–	Data bus input
berr	input	low	Bus error
dsi	input	–	BDM serial interface data input
dsclk/bkpt	input	low	BDM serial interface data clock input / breakpoint
dso	output	–	BDM serial interface data output
freeze	output	high	CPU is frozen by BDM
datao[15:0]	output	–	Data bus output
addr[23:0]	output	–	Address data bus
bg	output	low	Bus grant
as	output	low	Address strobe
rdwr	output	high/low	Read write signal
uds	output	low	Upper data byte strobe
lds	output	low	Lower data byte strobe
addrz	output	high	Turns Address bus into 'Z' state
dataz	output	high	Turns Data bus into 'Z' state
ctrlz	output	high	Turns as, rdwr, uds, lds, vma, fc(2:0) signals into 'Z' state
fc[2:0]	output	high	Processor function code
epd	output	high	Enable peripheral device
vma	output	low	Valid memory address
halto	output	low	Halt output
rsto	output	low	Reset output

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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