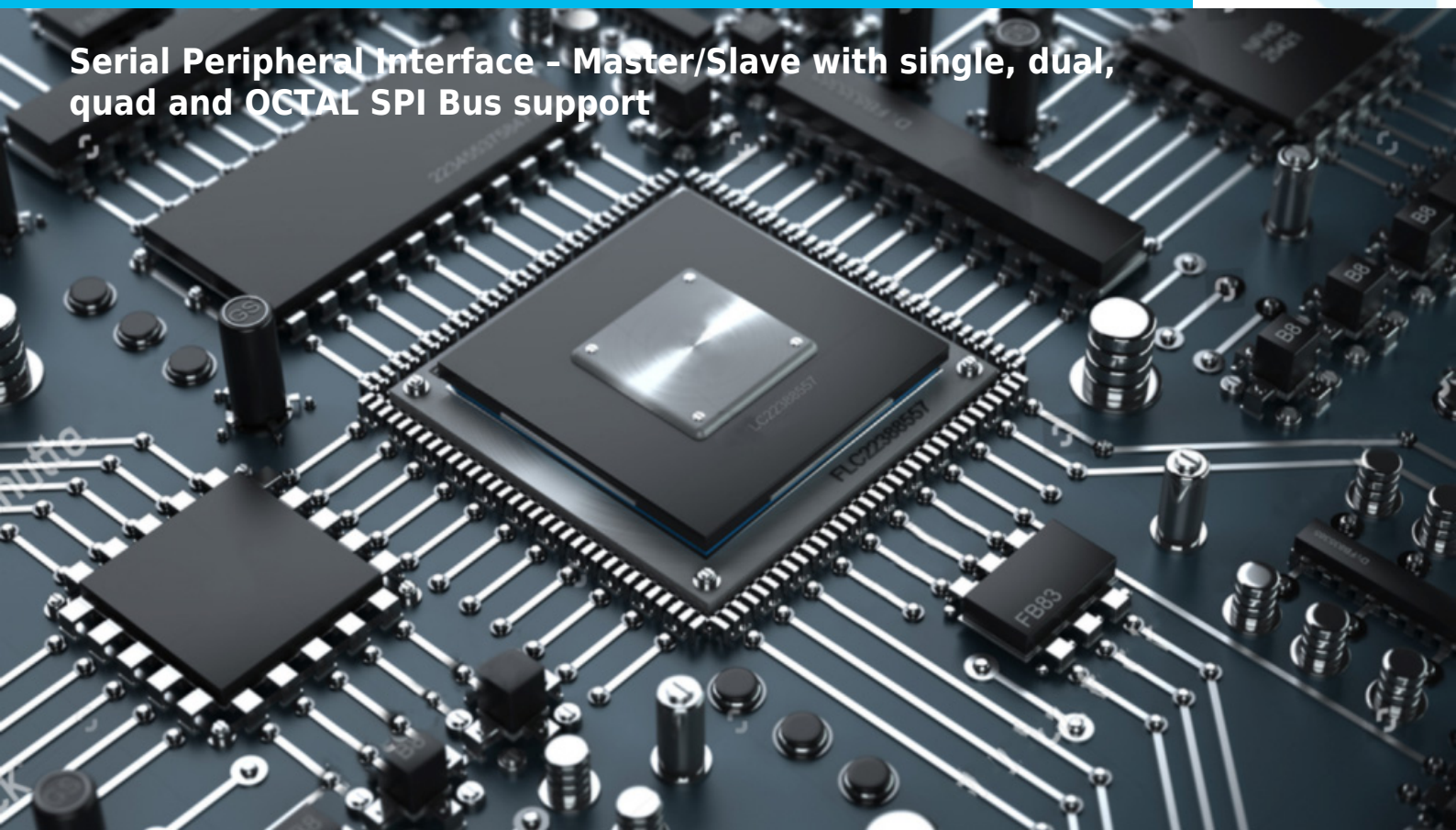
DIGITAL CORE DESIGN

DOSPI

Serial Peripheral Interface – Master/Slave with single, dual, quad and OCTAL SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DOSPI Octal SPI IP Core — High-Speed, Low-Latency SPI Controller for Advanced SoC & FPGA Designs

The **DOSPI Octal SPI IP Core** is a high-performance, low-latency SPI controller engineered for next-generation **SoC and FPGA architectures**. Designed for demanding embedded applications, the DOSPI delivers exceptional throughput and deterministic timing, providing **maximum SPI clock speeds up to CLK/2**—far beyond typical SPI controllers limited to **CLK/8**. This makes it an ideal choice for systems requiring **fast access to serial SPI memories**, high-bandwidth peripherals, or real-time inter-processor communication.

Fully compatible with **APB, AHB, and AXI** system buses, the DOSPI integrates seamlessly into a wide range of design environments. The core supports **8-, 16-, and 32-bit processors**, as well as **little-endian and big-endian** data formats, ensuring broad compatibility across embedded platforms. As a **programmable SPI Master/Slave**, it provides full control over **SCK polarity, phase**, and four advanced SPI clocking modes—guaranteeing interoperability with virtually any synchronous serial peripheral.

At the heart of the DOSPI is support for **Single, Dual, Quad, and Octal SPI** transfer modes. With **Double Data Rate (DDR)** clocking enabled, the IP core transfers data on **both edges of the SCK signal**, achieving up to **16 bits per SCK cycle in Octal DDR mode**. This level of performance is crucial for **high-speed SPI Flash**, **low-latency Execute-in-Place (XIP)** systems, **RAM shadowing**, and any design where startup time, code throughput, or memory bandwidth is essential.

Optimized for Performance-Critical Applications

The DOSPI Octal SPI IP Core excels in:

- **Execute-in-Place (XIP)** architectures requiring minimal latency
- Systems performing **fast Flash-to-RAM shadowing** or real-time memory access
- **Cost-optimized embedded platforms** requiring high performance without parallel memory buses
- **Inter-processor communication** in multi-master topologies
- Designs requiring **octal SPI flash support** and maximum bandwidth utilization

Robust Reliability & Multi-Master Safety

For complex bus environments, DOSPI integrates advanced protection mechanisms, including:

- **Write-collision detection**
- **Multi-master arbitration fault protection**
- **Automatic disabling of drivers during contention**
- **Deterministic slave selection** via the dedicated **Slave Select Control Register (SSCR)**

This ensures stable operation in systems with shared buses, multiple masters, or safety-critical workloads.

High-Efficiency DMA Support

The DOSPI supports **single-transfer** and **multi-transfer DMA modes**, enabling:

- Zero-CPU-overhead transfers
- Continuous high-speed streaming
- Efficient integration with **high-performance DMA controllers**

This is essential for designs that must sustain maximum data throughput while minimizing power and processing overhead.

Customizable, Technology-Independent Design

As with all **DCD-SEMI IP cores**, the DOSPI is:

- **Fully customizable** for specific SoC or FPGA requirements

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- **Technology-agnostic**, ready for ASIC or FPGA implementation

- Delivered with optional modifications for protocol, timing, and bus configurations

This flexibility ensures optimal fit for architectures focused on memory performance, boot-time reduction, or low-power embedded operation.

Why Engineers Choose DOSPI

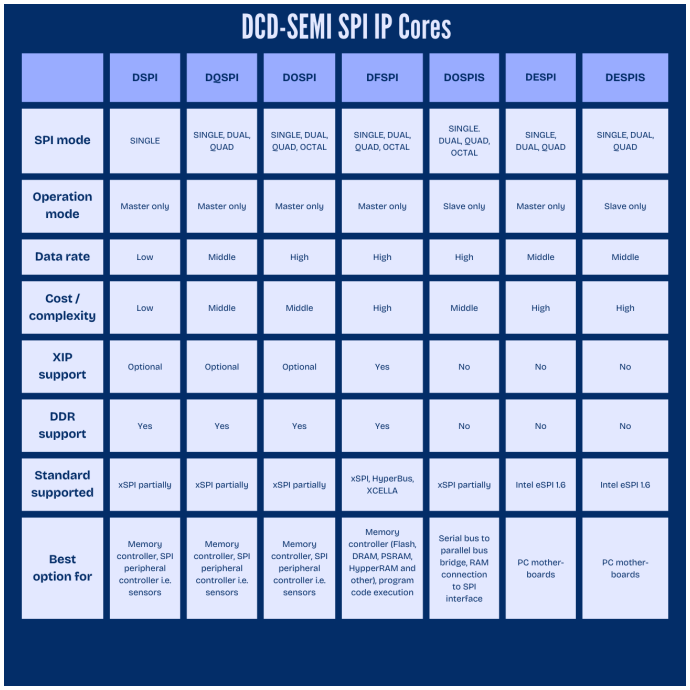
If your design requires **maximum SPI throughput**, **ultra-low latency**, advanced **Quad/Octal SPI support**, and seamless **APB/AHB/AXI** integration, the DOSPI Octal SPI IP Core delivers best-in-class performance for **next-generation embedded, automotive, industrial, and consumer SoC designs**.

Which One to Choose DQSPI vs DOSPI

Feature / Requirement	DQSPI (Quad SPI)	DOSPI (Octal SPI)	Which to choose?
Bus Width	1-bit (Single), 2-bit (Dual), 4-bit (Quad)	1-bit, 2-bit, 4-bit, **8-bit (Octal)**	If you need **max throughput**, choose **DOSPI**.
Max Data Throughput	Up to **8 bits per SCK** (Quad + DDR)	Up to **16 bits per SCK** (Octal + DDR)	DOSPI for high-bandwidth memory boot or XIP; DQSPI is optimal for mid-range.
Supported Protocols	Single, Dual, Quad SPI	Single, Dual, Quad, **Octal SPI**	DOSPI covers everything DQSPI does — and more.
DDR Support (Double Data Rate)	Yes (Dual & Quad)	Yes (Dual, Quad & Octal)	Both excellent for speed-critical systems.
Supported CPU Bus Widths	8 / 16 / 32-bit	8 / 16 / 32-bit	Both match common MCU/SoC designs.
Clocking Flexibility	Full control of SCK polarity, phase & protocols	Full control of SCK polarity, phase & protocols	Equal – both adaptable to any SPI memory.
Typical Use Cases	Quad-SPI NOR/NAND, XIP boot, mid-range SoCs	Octal-SPI NOR/NAND, ultra-fast XIP, high-end SoCs, performance-critical systems	Choose DQSPI for cost-optimized designs; DOSPI for high-end devices.
Interprocessor Communication	Yes	Yes	Same functionality.
DMA Support	Single & multi-transfer modes	Single & multi-transfer modes	Same — both integrate with high-performance DMA.
Master/Slave Mode	Both supported	Both supported	Same.
Performance Advantage	Data rate up to **CLK/2**	Data rate up to **CLK/2** (vs typical market CLK/8)	Both outperform competitors; DOSPI achieves highest bandwidth.
Best Match For	Mid-range embedded systems, cost-sensitive devices, Quad-SPI flash	High-performance designs, fast booting, real-time apps, Octal flash	Engineers optimize cost → DQSPI, optimize speed → DOSPI.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.



- Operates with 8, 16 and 32 bit CPUs
- Full duplex synchronous serial data transfer
- DMA support
- Support for 32, 16 and 8 bit systems
- Support for various system Bus Standards
- Single, Dual, Quad and Octal SPI transfer
- DDR support (Double Data Rate)
- Multimaster system supported
- Optional FIFO size extension (128, 256, 512B)
- Up to 7 SPI slaves can be addressed (more Slave Select Outputs can be added upon request)
  - Software Slave Select Output – SSO - selection
  - Automatic Slave Select outputs assertion during each byte transfer
- System error detection
- Interrupt generation
- Various Bit rates supported
- Bit rate in fast SPI Mode ½ CLK
- Four transfer formats
- Simple CPU and DMA interface
- Fully synthesizable, static synchronous de-sign with no

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PERFORMANCE

For precise ASIC performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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