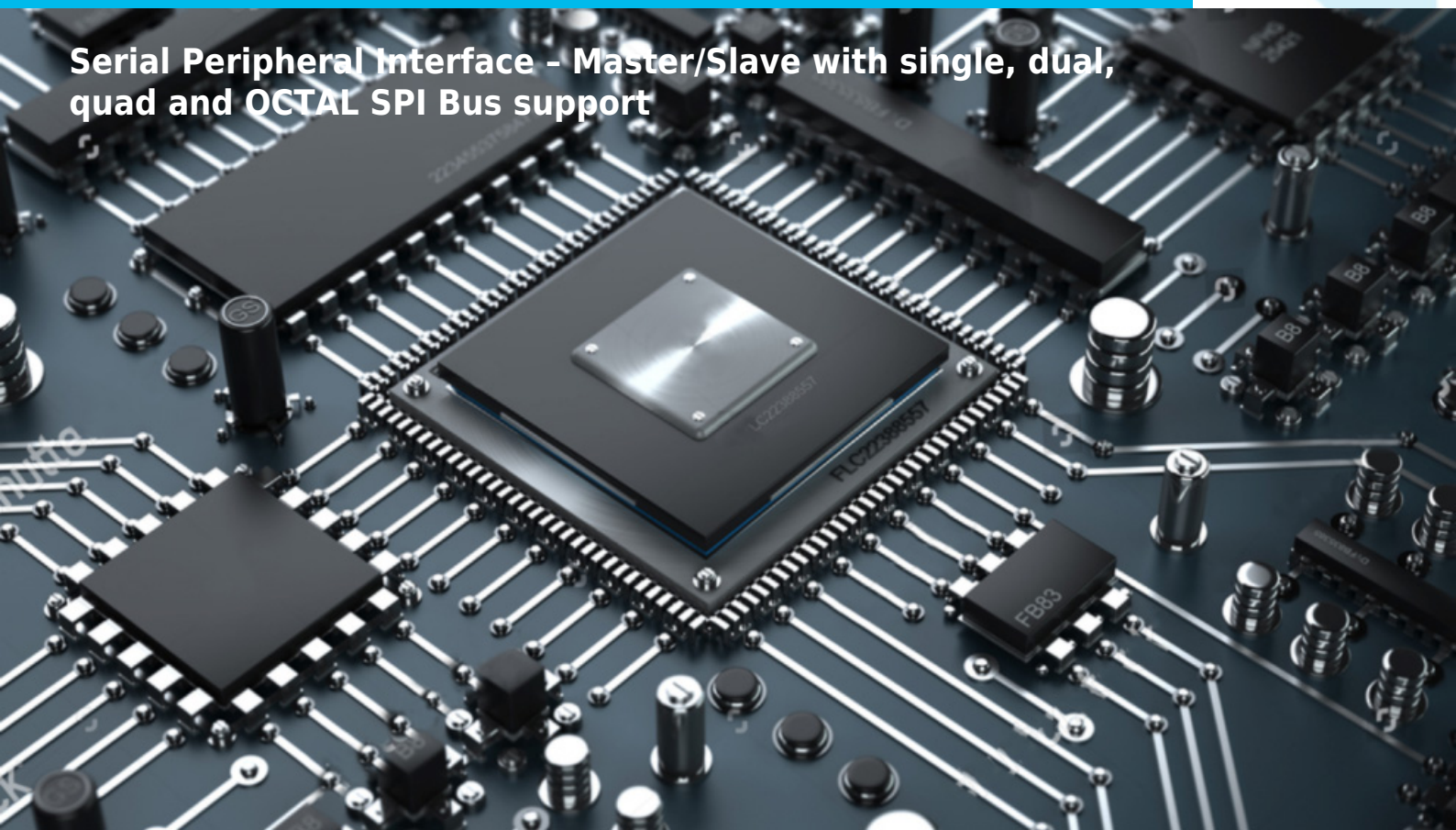
DIGITAL CORE DESIGN

DOSPI

Serial Peripheral Interface – Master/Slave with single, dual, quad and OCTAL SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DOSPI bridge to APB, AHB, and AXI bus, it is a revolutionary **octal SPI** designed to offer **the fastest operations available for any serial SPI memory**.

It is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Moreover, the IP Core **supports all 8, 16, and 32-bit processors** available on the market. The DOSPI is a fully configurable SPI master/slave device, which allows you to configure the polarity and phase of serial clock signal SCK. It enables the microcontroller to communicate with **fast serial SPI memories** and **serial peripheral devices**. Moreover, it's capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes the shifting and sampling of information on four serial data lines. In the **Single** SPI mode, data is simultaneously transmitted and received, while in **DUAL**, **QUAD, and OCTAL** SPI modes, data is shifted in or out respectively on two, four, and eight data lines at once. Additionally, transfer speed can be doubled by using the **DDR protocol** (Double Data Rate) – This feature allows the DOSPI to transfer/receive data on both falling and rising edges of SCK. The DDR together with OCTAL SPI transfer allows 8 bits of data to be sent/received within a single SCK clock cycle. This makes the DOSPI perfect for systems, where performance is essential, or where the code can be moved from non-volatile memory to fast RAM, for systems where device size and cost are the keys, or where the program code can be executed directly from non-volatile memory, using an approach known as **Execute-in-Place**. DCD's IP Core is a **technology-independent** design that can be implemented in a variety of process technologies. The DOSPI system is flexible enough to **interface directly with numerous standard product peripherals from several manufacturers**. The system can be configured as a master or slave device. **Data rates are as high as CLK/2** when other vendors' solutions offer just CLK/8. Clock control logic allows selecting clock polarity, phase, and four fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, the software selects bit rates for the serial clock. The DOSPI automatically drives selected by SSCR (Slave Select Control Register) slave select outputs (SS7O – SS0O), and addresses the SPI slave device to exchange serially shifted data. **Error-detection logic** is included, to support interprocessor communications. A **write-collision detector** indicates when an attempt is made to write data to the serial shift register, while the transfer is in progress. A **multiple-master mode-fault detector** disables DOSPI output drivers automatically if more than one SPI device simultaneously attempts to become a bus master. The **DOSPI supports two DMA modes: single transfer and multi-transfer**. These modes allow the DOSPI to interface to higher performance DMA units which can interleave their transfers between CPU cycles or execute multiple byte transfers. The DOSPI is fully customizable – it is delivered in the exact configuration to meet your requirements.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

- Operates with 8, 16 and 32 bit CPUs
- Full duplex synchronous serial data transfer
- DMA support
- Support for 32, 16 and 8 bit systems
- Support for various system Bus Standards
- Single, Dual, Quad and Octal SPI transfer
- DDR support (Double Data Rate)
- Multimaster system supported
- Optional FIFO size extension (128, 256, 512B)
- Up to 7 SPI slaves can be addressed (more Slave Select Outputs can be added upon request)
  - Software Slave Select Output – SSO - selection
  - Automatic Slave Select outputs assertion during each byte transfer
- System error detection
- Interrupt generation
- Various Bit rates supported
- Bit rate in fast SPI Mode ½ CLK
- Four transfer formats
- Simple SPU and DMA interface
- Fully synthesizable, static synchronous de-sign with no internal tri-states
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

PERFORMANCE

To provide you with the most accurate and detailed insights

about the Lattice performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– ***Single-Site license option*** – dedicated to small and middle sized companies which run their business at one place.

– ***Multi-Site license option*** – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited.

There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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