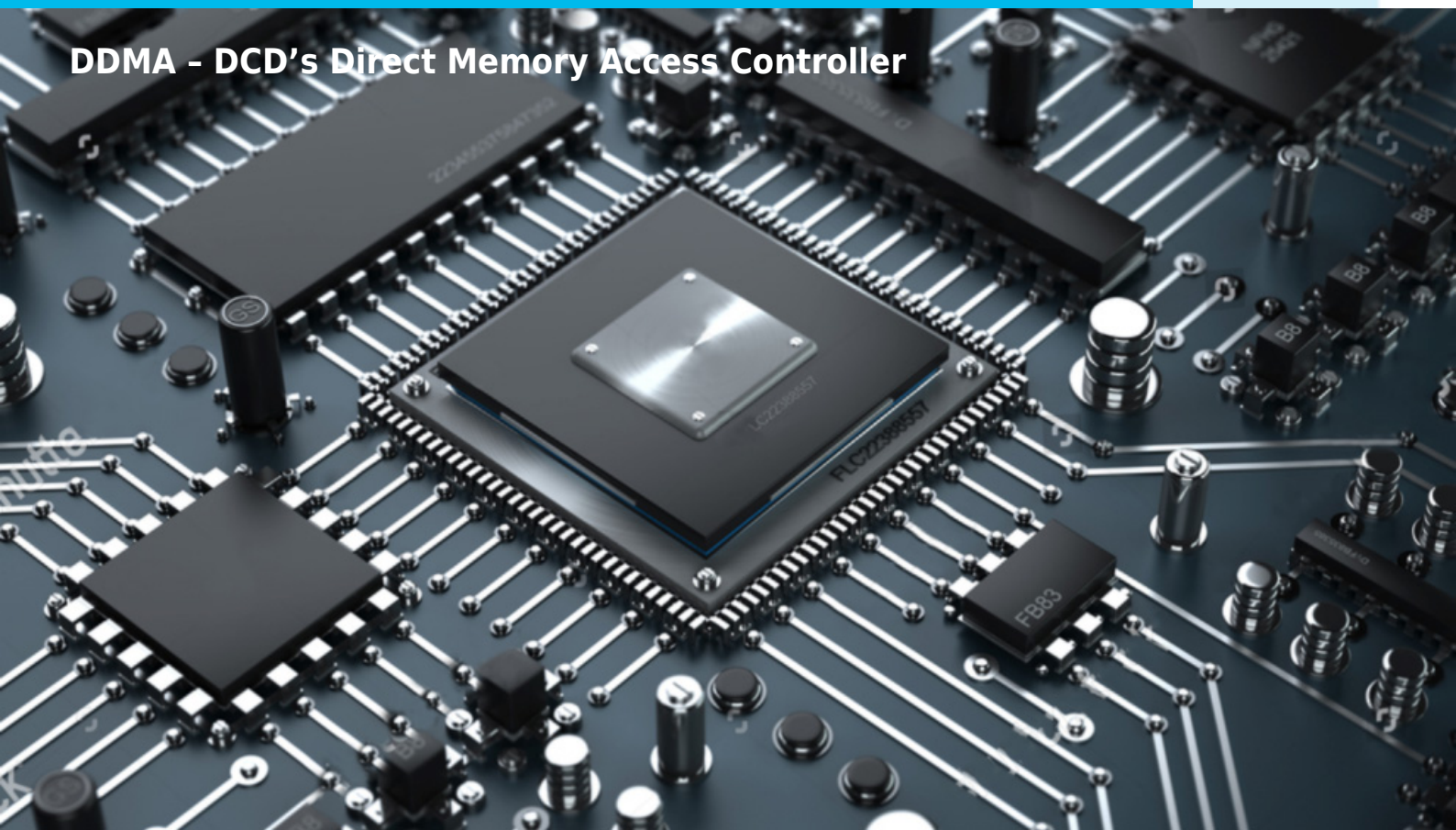
DIGITAL CORE DESIGN

DDMA, DIRECT MEMORY ACCESS



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DDMA IP Core — High-Performance Four-Channel Direct Memory Access Controller

Efficient Data Transfer for CPU-Offloading and System Performance

The **DDMA IP Core** from DCD-SEMI is a **four-channel Direct Memory Access (DMA) controller** designed to optimize **data transfers between memory and peripherals**, significantly reducing CPU load and improving system performance in **embedded systems**, **SoCs**, and **FPGA designs**.

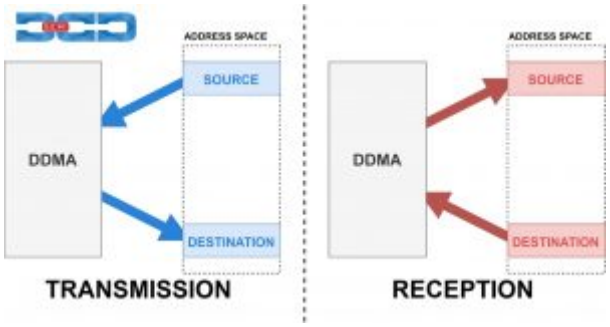
Programmed via a **32-bit or 8-bit native interface**, the DDMA supports configurable **data transaction sizes** across a **32-bit address space**, ranging from **1 byte up to 16 MB per transaction**. To ensure smooth operation across peripherals with varying timing characteristics, the DDMA features a **32-bit FIFO transfer buffer** with configurable depth.

Flexible Triggering and Peripheral Request Interface

Data transactions can be initiated by either **hardware or software triggers**:

- **Hardware Trigger:** Utilizes the **Peripheral Request Interface (PRI)**, enabling external peripherals to request data transmission or reception on a specific DDMA channel.
- **Software Trigger:** Managed by the CPU through channel registers.

When multiple channels request transfers simultaneously, the DDMA employs a **round-robin arbitration algorithm** to efficiently manage channel priorities.



Four Independent Channels

The DDMA includes **four configurable channels**, each with dedicated **configuration registers**, **enable bits**, and **status flags**. Each channel supports **three transfer modes**:

- **SINGLE:** Transfers a single data item per request
- **NORMAL:** Transfers one block of data per request
- **BLOCK:** Transfers all configured data blocks per request

Data blocks can be customized in **byte size and number of blocks**, and each channel supports **8-, 16-, and 32-bit read/write operations**, independently configurable for **source and destination**.

Flexible Addressing and Reload Options

The DDMA provides **three addressing modes**:

- **INC:** Increment address after each access
- **DEC:** Decrement address after each access
- **FIXED:** Maintain the same address

Additionally, it offers **three source and destination address reload options**:

- **TRANSACTION:** Reload after full transaction
- **BLOCK:** Reload after each block transfer
- **NEVER:** No reload

All address, block, and byte registers are **double-buffered**, ensuring that updates during active transfers only take effect after the current operation completes.

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Advanced Status Flags and Interrupts

Each DDMA channel features **channel status flags** (**BUSY**, **PENDING**, **IDLE**) and **transfer status flags** to track the amount of data transmitted. Transfer status flags are maskable, allowing the generation of **interrupts** for specific transfer conditions, enhancing **system responsiveness** and **control for real-time applications**.

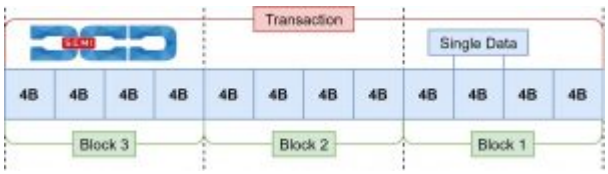
Why Choose DCD-SEMI DDMA IP Core

- **Four independent DMA channels** with dedicated registers and FIFO buffers
- **Configurable transfer sizes** from 1 byte to 16 MB
- **Supports 8-, 16-, and 32-bit read/write operations**
- **Flexible addressing and reload modes** for source and destination
- **Hardware and software triggers with round-robin arbitration**
- **Maskable transfer status flags for interrupt generation**
- Ideal for **high-performance embedded systems, SoCs, and FPGA designs**

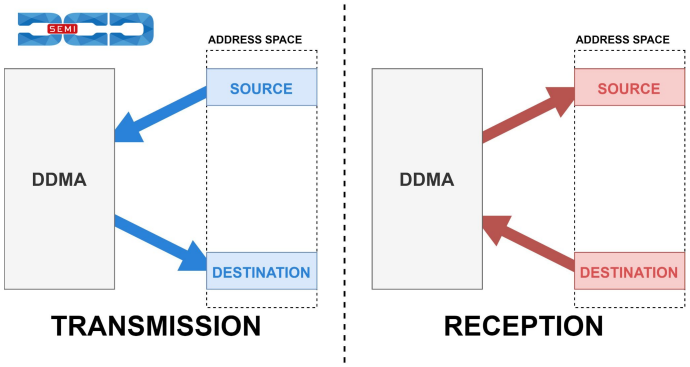
ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For technical details, integration support, or customization options, contact **info@dcd-semi.com**

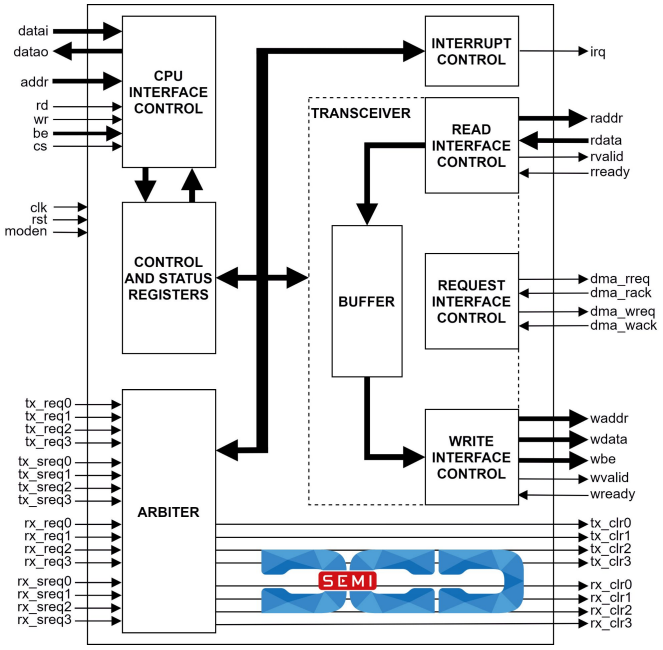
CONFIGURATION



BLOCK DIAGRAM



SYMBOL



PERFORMANCE

For precise ASIC performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users

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to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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