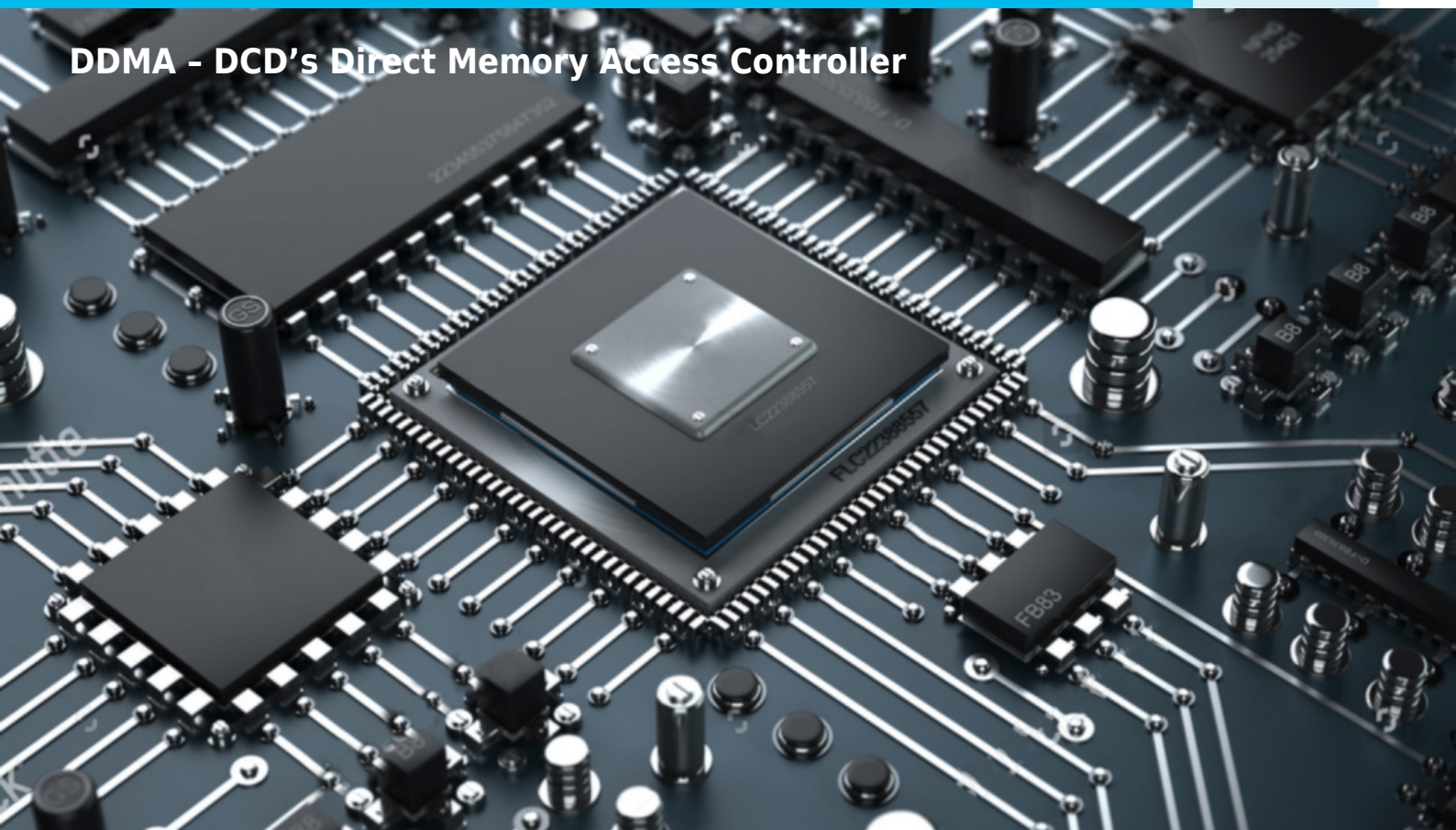
DIGITAL CORE DESIGN

DDMA, DIRECT MEMORY ACCESS CONTROLLER



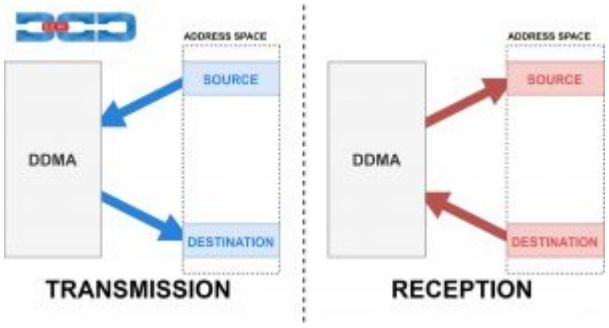
COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DDMA is a four-channel Direct Memory Access Controller. Its purpose is to transfer data between memories and peripherals to *reduce CPU utilization* during data transfers. It can be programmed by the CPU via a 32-bit or 8-bit native interface. The DDMA can perform **data transactions of configurable size over 32-bit address space**. A single transaction size can be set in a range from 1B to 16MB. To limit the negative impact of different reads and writes timing the DDMA features transfer data buffer. This buffer is a **32-bit FIFO memory with configurable depth**.

Data transactions can be triggered either by hardware or software. Hardware initialization is achieved via the *Peripheral Request Interface*, while software initialization is done by the *CPU via registers*. The Peripheral Request Interface is used by external controllers (peripherals) to set data transaction requests on specific DDMA channel. Each of the DDMA channels has a set of Peripheral Request Interface signals associated with it. Peripherals can request the transmission or reception of data. When multiple channels await data transfer the arbitration process utilizes a round-robin algorithm.



There are four DDMA channels. Each has its configuration registers and enable bit.
The DDMA offers three transfer modes:

1. SINGLE – single data transfer on request,
2. NORMAL – one data block transfer on request,
3. BLOCK – all data blocks transfer on request.

They are distinguished by the amount of data transferred on a single request. Data transaction is divided into blocks. It is possible to configure the number of block bytes and blocks in a transaction. Data transfer is performed between the data source and the data destination. **The DDMA channel can perform reads and writes on 32-bit, 16-bit, and 8-bit data** which is separately configurable for both source and destination. Source and destination addresses can be freely configured.

The DDMA offers **three addressing modes:**

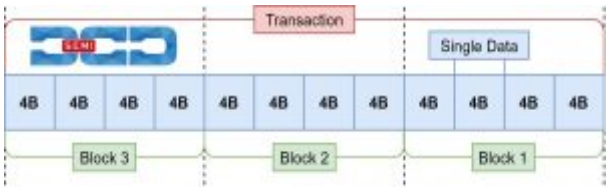
1. INC – increment address after each data access,
2. DEC – decrement address after each data access,
3. FIXED – the address is fixed.

Apart from the above, the IP Core has t**hree sources and destination address reload options:**

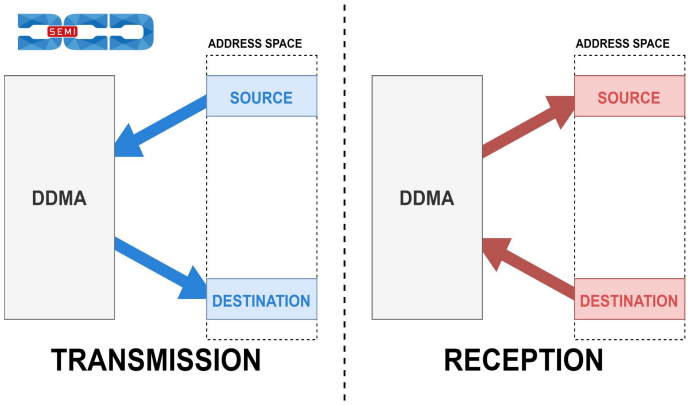
1. TRANSACTION – address is reloaded after the full transaction,
2. BLOCK – the address is reloaded with each block transferred,
3. NEVER – the address is never reloaded.

Address, block, and byte registers are double-buffered so that if they are changed while the channel is busy, the change does not take effect until the current data transfer is over.

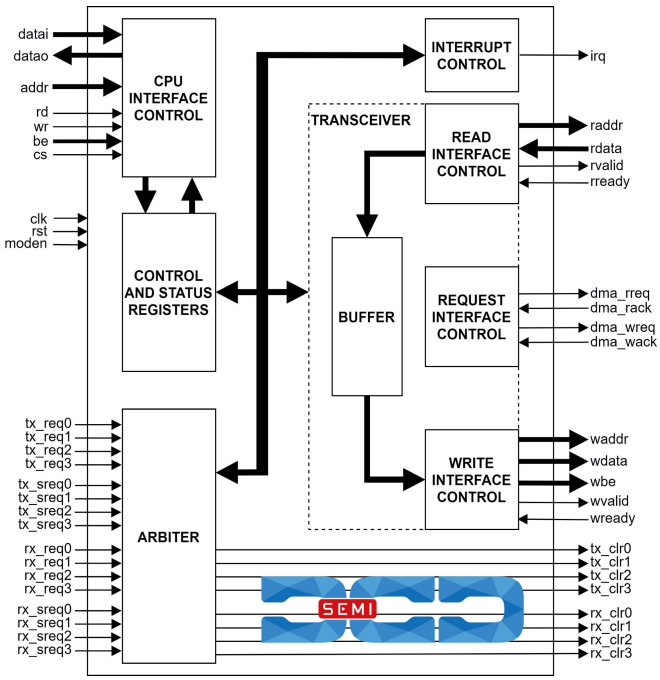
Each channel has status and transfers status flags. **Channel status is defined as BUSY, PENDING, or IDLE**. Transfer status flags inform about the amount of data that has been sent by the channel. Proper flags are set after transmitting a single data, block, or transaction. Each transfer status flag is masked which allows for generating an interrupt request when a specific data transfer situation occurs.



BLOCK DIAGRAM



SYMBOL



PERFORMANCE

To provide you with the most accurate and detailed insights about the Xilinx performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/