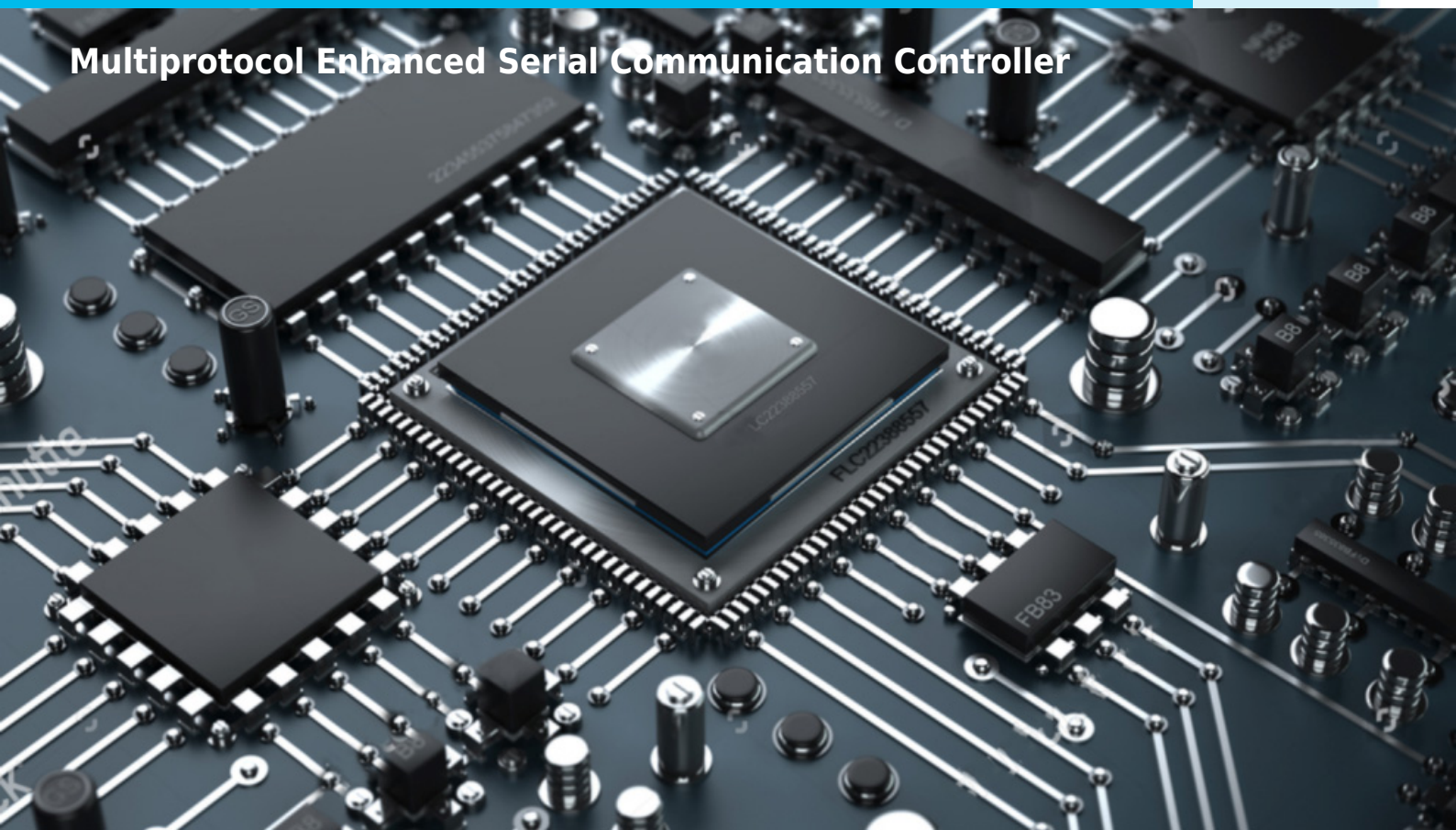
DIGITAL CORE DESIGN

DMESCC

Multiprotocol Enhanced Serial Communication Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DMESCC – **Dual channel Multiprotocol Enhanced Serial Communication Controller**, is designed for use with 8- and 16- bit microprocessors.
DMESCC handles asynchronous formats, synchronous byte-oriented protocols such as **IBM® Bisync**, and synchronous bit-oriented protocols such as **HDLC** and **SDLC**. The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The DMESCC also has facilities for modem control in both channels.

The user can configure DMESCC to handle all asynchronous formats regardless of data size, number of stop bits, or parity requirements. Control is done through the number of control and status registers for each channel separately. Within each operating mode, the DMESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.
The ultimate functionality of DMESCC denotes its usability:

- **as a data communications device**, DMESCC transmits and receives data in a wide variety of data communication protocols.
- **as a microprocessor peripheral**, it offers valuable features such as vectored interrupts, polling, and simple handshake capability.

DMESCC provides two independent full-duplex channels, programmable for use in any standard asynchronous or synchronous data communication protocol. In Asynchronous mode transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-half, or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU.

DESIGN FEATURES:

All DCD's IP Cores are technology independent which means that they are 100% compatible with all FPGA & ASIC vendors e.g.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Dual-Channel: A, B
- Configuration capability
- **Asynchronous mode**:
  - Asynchronous (x16, x32, or x64 clock
  - Isochronous (x1 clock)
- **Character-Oriented mode**:
  - Monosynchronous
  - Bisynchronous
  - External Synchronous
- **Bit-Oriented mode**:
  - ◊ SDLC/HDLC
  - ◊ SDLC/HDLC Loop
- Complete status reporting capabilities
- Receiver data FIFO and Error FIFO
- SDLC Frame FIFO
- Transmitter FIFO
- **Data encoder\decoder**:
  - NRZ, NRZI
  - FM0, FM1
  - Manchester (require external logic)
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Auto Echo
  - Break, parity, overrun, framing error simulation
- Fully synchronous design with no internal tri-state buffers

Transmission modes:

- Synchronous Byte (Bisync) features
  - 5 to 8 Bit characters
  - Programmable Sync character
  - Transparent text mode operation
  - Automatic Sync insertion during Idle
  - Hardware CRC generation and detection
  - CRC-16 or CRC-CCITT polynomials
- Asynchronous Features
  - 5-8 Bits per character
  - 1, 1,5, and 2 stop bits
  - Break generation and detection
  - Parity, overrun, and framing error detection
  - Even, Odd or no parity
- Modem controls and indicators

- CTS and DCD lines, usable for modem control or user-defined input
- DTR and RTS usable for modem control or user-defined output

- Synchronous SDLC features
  - 1-8 Bits character (transmitter)
  - 5-8 Bits receiver character
  - Hardware address recognition
  - Automatic zero insertion and deletion
  - I-Field residue handling
  - Automatic flag insertion between messages
  - Hardware CRC generation and reception
- Interrupt system features
  - Channel functions and timers internally prioritized
  - Channel functions and timers generate unique interrupt mode
  - Prioritized Daisy-chain.
- LOOPBACK test mode

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA	2 033/943	608	83 MHz
ARIA II	1 954/943	608	167 MHz
ARIA V	1 966/1 052	608	118 MHz
CYCLONE	2 730	608	68 MHz
CYCLONE II	2 883	608	90 MHz
CYCLONE III	2 896	608	109 MHz
CYCLONE IV E	2 869	608	112 MHz
CYCLONE IV 6X	2 881	608	112 MHz
CYCLONE V	1 967	608	89 MHz
STRATIX	2 730	608	72 MHz
STRATIX II	2 037	608	123 MHz
STRATIX III	1 962/997	608	214 MHz
STRATIX IV	1 952/997	608	196 MHz
STRATIX V	1 950/1 044	608	219 MHz
MAX 10	2 935	608	90 MHz

DELIVEVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF Netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core updates, minor and major versions changes
    - Delivery of the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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