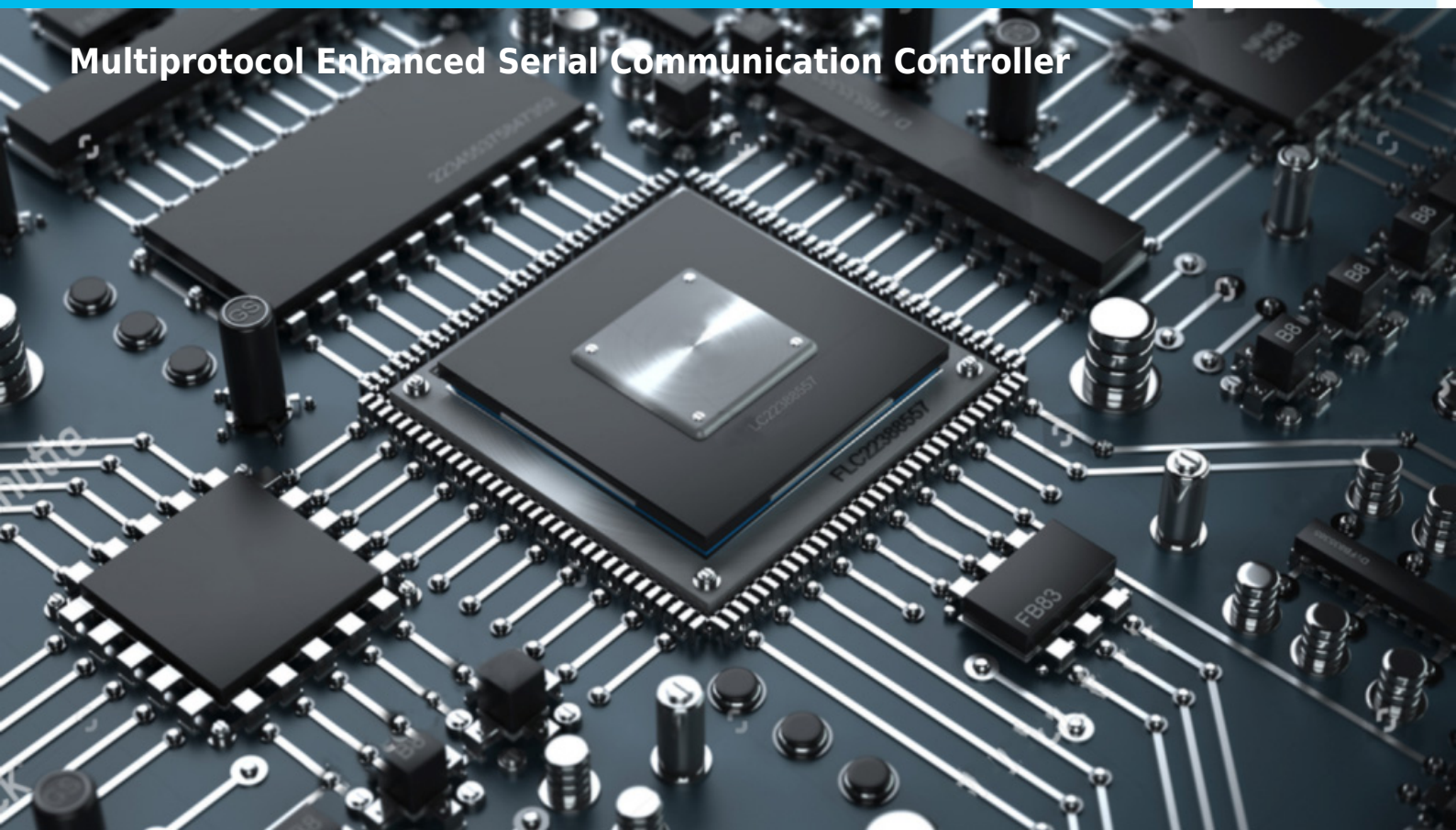
DIGITAL CORE DESIGN

DMESCC

Multiprotocol Enhanced Serial Communication Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DMESCC IP Core – Dual-Channel Multiprotocol Serial Controller for FPGA & ASIC

The **DMESCC IP Core** from **DCD-SEMI** is a **Dual-Channel Multiprotocol Enhanced Serial Communication Controller** designed for reliable integration into **FPGA and ASIC designs**. Optimized for use with **8-bit and 16-bit microprocessors**, DMESCC provides a flexible and scalable solution for implementing both **asynchronous and synchronous serial communication protocols** in embedded, industrial, and telecommunications systems.

With two fully independent full-duplex channels, DMESCC enables simultaneous transmit and receive operations, ensuring deterministic performance across a wide range of serial data transfer applications.

Broad Protocol Support

DMESCC supports a comprehensive set of serial communication formats, including:

- **Asynchronous serial protocols**
- **Synchronous byte-oriented protocols** (e.g. **IBM® Bisync**)
- **Synchronous bit-oriented protocols**, such as **HDLC** and **SDLC**

In all synchronous modes, the IP Core can **generate and check CRC codes**, allowing designers to implement robust data integrity checking tailored to application-specific requirements.

Highly Configurable Serial Operation

Each channel of the DMESCC IP Core is independently configurable through dedicated **control and status registers**, enabling fine-grained protocol control. The core supports:

- Variable **data sizes** (5 to 8 bits per character)
- Programmable **odd or even parity**
- **One, one-and-a-half, or two stop bits**
- **Character insertion and deletion**
- **Break and abort generation and detection**
- Flexible **CRC generation and checking**

This configurability allows DMESCC to adapt to both **legacy communication standards** and modern embedded designs without hardware changes.

Dual-Channel Full-Duplex Architecture

DMESCC provides **two independent full-duplex channels**, each programmable for any supported asynchronous or synchronous protocol. In asynchronous mode, transmission and reception can operate independently per channel, while built-in **break generation and break-detection logic** enables immediate CPU notification via interrupts when exceptional conditions occur.

Microprocessor-Friendly Features

When used as a microprocessor peripheral, DMESCC offers valuable system-level capabilities, including:

- **Vectored interrupts**
- **Polling support**
- **Simple handshake mechanisms**
- **Modem control on both channels**

These features simplify firmware design and improve responsiveness in real-time systems.

Typical Applications

- Telecommunications equipment
- Industrial automation systems
- Embedded controllers

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- Legacy protocol implementations

- FPGA-based SoCs requiring multiprotocol serial I/O

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Dual-Channel: A, B
- Configuration capability
- **Asynchronous mode**:
  - Asynchronous (x16, x32, or x64 clock
  - Isochronous (x1 clock)
- **Character-Oriented mode**:
  - Monosynchronous
  - Bisynchronous
  - External Synchronous
- **Bit-Oriented mode**:
  - ◊ SDLC/HDLC
  - ◊ SDLC/HDLC Loop
- Complete status reporting capabilities
- Receiver data FIFO and Error FIFO
- SDLC Frame FIFO
- Transmitter FIFO
- **Data encoder\decoder**:
  - NRZ, NRZI
  - FM0, FM1
  - Manchester (require external logic)
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Auto Echo
  - Break, parity, overrun, framing error simulation
- Fully synchronous design with no internal tri-state buffers

Transmission modes:

- Synchronous Byte (Bisync) features
  - 5 to 8 Bit characters
  - Programmable Sync character
  - Transparent text mode operation
  - Automatic Sync insertion during Idle
  - Hardware CRC generation and detection
  - CRC-16 or CRC-CCITT polynomials
- Asynchronous Features
  - 5-8 Bits per character
  - 1, 1,5, and 2 stop bits
  - Break generation and detection
  - Parity, overrun, and framing error detection
  - Even, Odd or no parity
- Modem controls and indicators
  - CTS and DCD lines, usable for modem control or user-defined input
  - DTR and RTS usable for modem control or user-defined output
- Synchronous SDLC features
  - 1-8 Bits character (transmitter)
  - 5-8 Bits receiver character
  - Hardware address recognition
  - Automatic zero insertion and deletion
  - I-Field residue handling
  - Automatic flag insertion between messages
  - Hardware CRC generation and reception
- Interrupt system features
  - Channel functions and timers internally prioritized
  - Channel functions and timers generate unique interrupt mode
  - Prioritized Daisy-chain.
- LOOPBACK test mode

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD** devices after Place & Route:

Device	LUTs /Slices	Mem. Blocks	F_{max} MHz
Artix 7	1 785/797	2	165
Kintex Ultra Scale	1 754	2	330
Kintex 7	1 877/676	2	239
Zynq 7000	1 816	2	330
Zynq	1 868/774	2	171
Virtex Ultra Scale	1 752	2	330
Virtex 7	1 869/878	2	194
Virtex 6	1 801/850	2	144
Virtex 5	1 861/846	2	161
Virtex 4	2 533/1 598	2	121
Spartan 6	1 815/681	2	122
Spartan 3E	2 647/1 655	2	75
Spartan 3	2 625/1 645	2	72

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods

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without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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