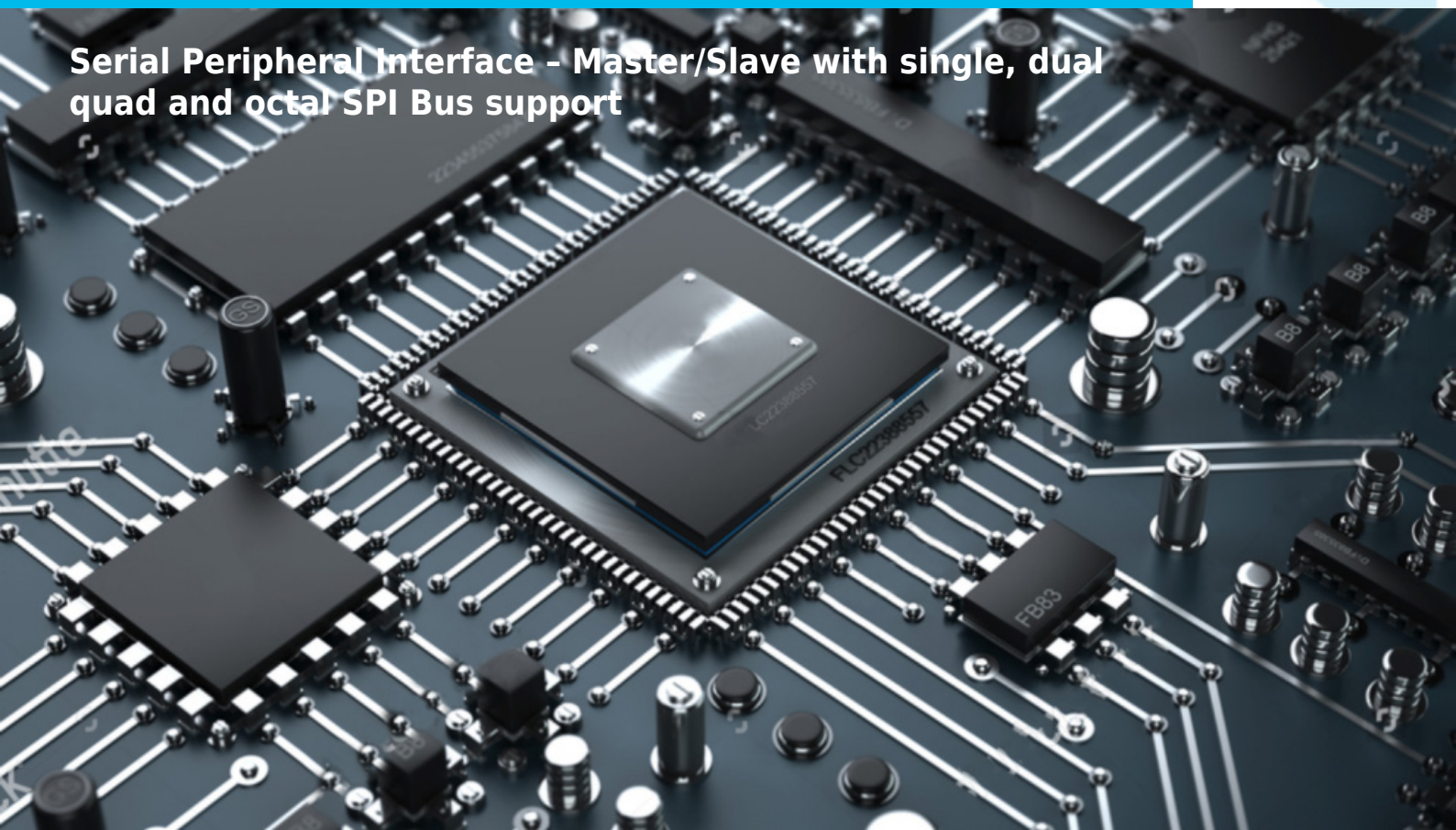
DIGITAL CORE DESIGN

DESPI

Serial Peripheral Interface – Master/Slave with single, dual quad and octal SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The **DESPI is a fully configurable eSPI master/slave device** supporting all features described in Enhanced Serial Peripheral Interface Base Specification rev. 1.0. The **DESPI master** is to be used by the microcontroller to communicate with eSPI peripheral devices. The **DESPI slave** is to be used as an eSPI peripheral device, e.g. an Embedded Controller attached to the Intel CPU system.

The **eSPI bus is an LPC bus improvement**. The serial clock line (_sck) synchronizes shifting and sampling of the information on the IO lines. It is a technology-independent design that can be implemented in a variety of process technologies. The DESPI is flexible enough to interface directly with numerous peripherals. The system might be configured as well as master as slave. Depending on the core configuration, the _in or _out lines are utilized. The serial clock may be up to 66MHz. The DESPI is also capable of simple, dual, and quad SPI transfers. The DESPI is fully customizable, which means it is delivered in the exact configuration meeting users' requirements. Additionally, the **DESPI module is equipped with receiver and transmitter FIFOs able to store up to 4096+16 bytes** (header and data payload or separate buffers for every eSPI channel and for posted/non-posted transfers), a customizable Peripheral Channel Memory and IO port, Virtual Wire lines and event lines.

The controller is capable to operate in several eSPI configurations: Single Master- Single Slave, Single Master – Multiple Slaves.

DESIGN FEATURES:

All DCD's IP Cores are technology independent which means that they are 100% compatible with all FPGA & ASIC vendors e.g.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix***

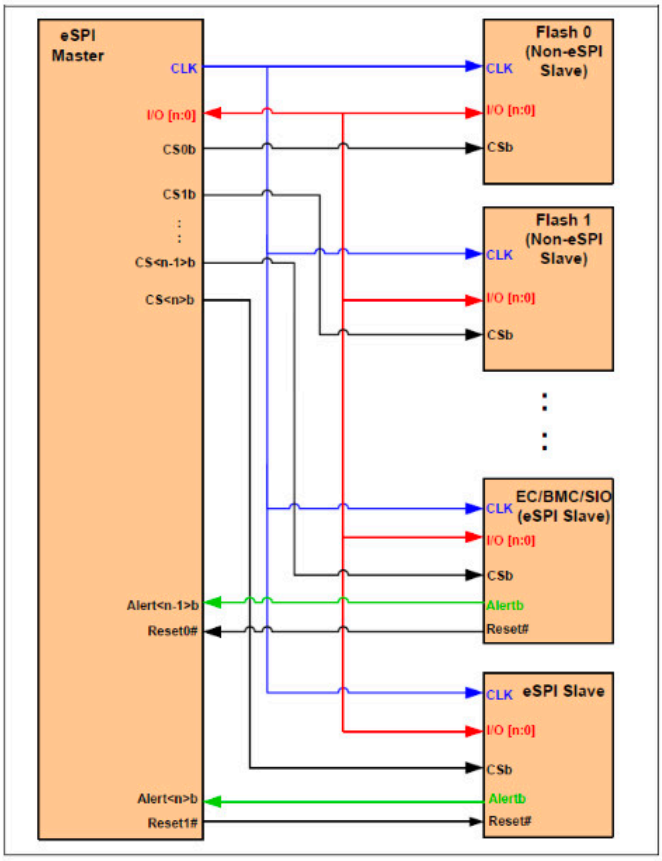
KEY FEATURES

- Compliant with eSPI base specification as defined in Enhanced Serial Peripheral Interface (eSPI) Specification rev.1.0
  - Supports Master and Slave Modes
  - Supports Single, Dual and Quad modes
  - Supports TX and RX operation as per specs
  - Support for
    - Command Phase
    - Turn-Around Phase
    - Response Phase
  - Baud Rate selection
  - Slave Triggered Transactions
  - Power management Event
  - Interrupts and Alerts
  - In-band reset
  - Support for multiple channels
    - Peripheral channel
    - Virtual wire Channel
    - OOB Message (Tunneled SMBus) Channel
    - Run-time Flash Access Channel
  - Various Master/Slave errors detection
  - CRC Checking and generation
  - Simple interface allows easy connection to microcontrollers
  - Fully synthesizable, static synchronous design with no internal tri-states
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core performance in **INTEL FPGA®** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	Memory Bits	F_{max}
ARIA GX	-6	287/201	1 024	158 MHz
ARIA 10	-1	371	1 024	327 MHz
CYCLONE	-6	382	1 024	152 MHz
CYCLONE2	-6	387	1 024	186 MHz
CYCLONE3	-6	375/200	1 024	234 MHz
CYCLONE4	-6	375/200	1 024	217 MHz
CYCLONE5	-6	288/200	1 024	187 MHz
MAX 10	-6	633	1 024	133 MHz
STRATIX	-5	382	1 024	167 MHz
STRATIX2	-3	289	1 024	314 MHz
STRATIX3	-2	300/242	1 024	408 MHz
STRATIX4	-2	290/240	1 024	360 MHz
STRATIX5	-2	307/212	1 024	375 MHz
STRATIX GX	-5	382	1 024	180 MHz
STRATIX2 GX	-3	288/201	1 024	254 MHz

DELIVEVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - EDIF Netlist
- VHDL or VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support

- IP Core implementation support 3 months of maintenance

  Delivery of the IP Core updates, minor and major version changes Delivery the documentation updates Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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