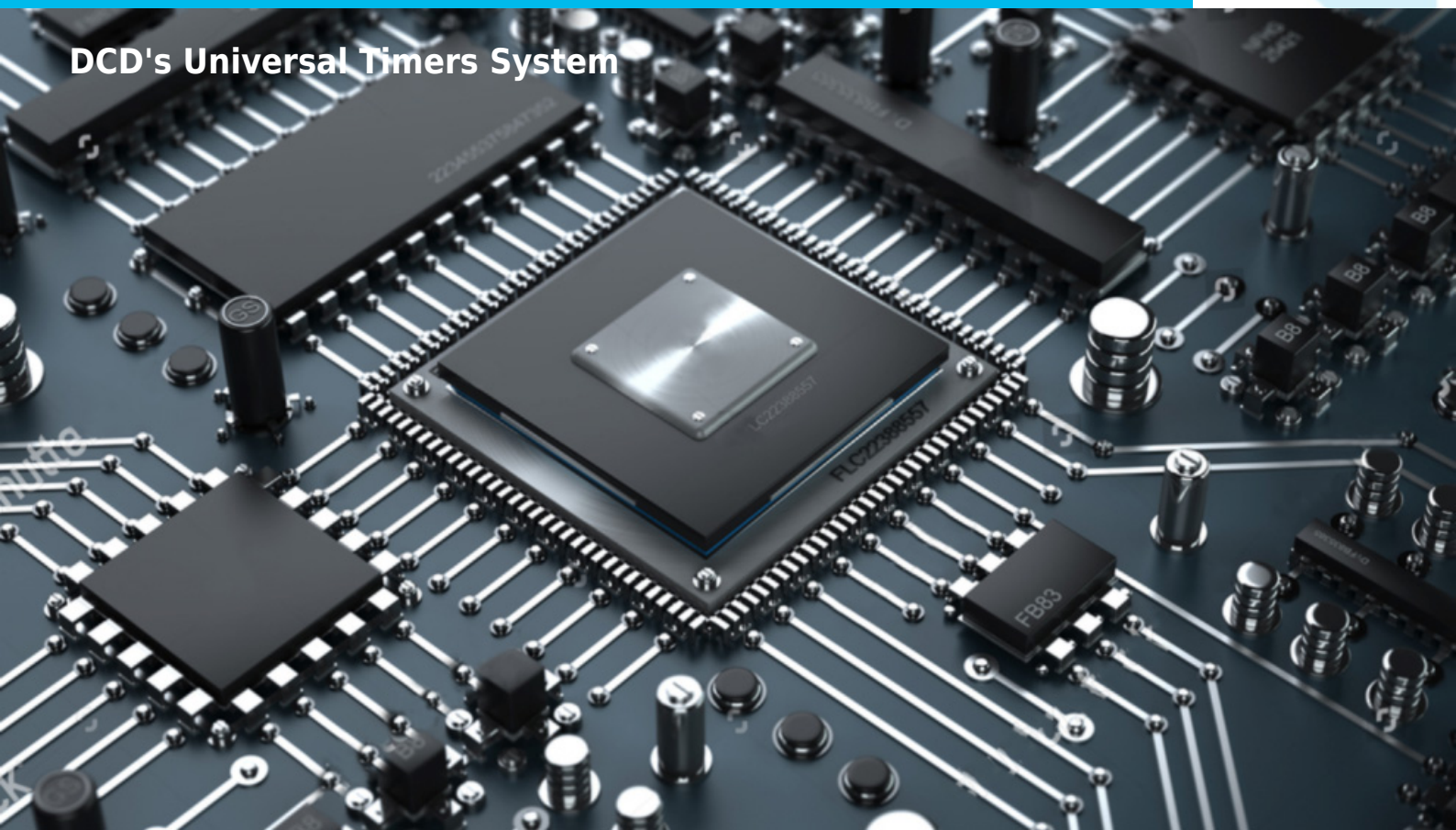
DIGITAL CORE DESIGN

DUTS



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The **DUTS** stands for **D**CD's **U**niversal **T**imers **S**ystem. It is a programmable and highly configurable device that comprises seven submodules:

- Pulse Width Modulation (PWM)
- Timer 1
- Timer 2
- Timer 3
- Real-Time Interrupt (RTI)
- Computer Operates Properly (COP)
- Pulse Accumulator (PA)

Each of these standalone modules provides **useful functionalities** which enable many design possibilities. Furthermore, if some module is not being used, it is possible to exclude it from design via one parameter. Moreover, in the case of the Timer 1 submodule, **it is possible to exclude single Output-Compare or Input-Capture function logic when it is not used**. This enables the minimization of hardware resources utilization. Moreover, users can **switch between 8-bit and 32-bit DUTS native interfaces**.

The **PWM timer subsystem** provides up to four 8-bit pulse width modulated channels. Channel pairs can be concatenated to create 16-bit PWM outputs. Three clock sources (A, B, and S) and a flexible clock select scheme give the PWM a wide range of frequencies. The user can determine each channel's polarity. Double buffered period and duty cycle registers for each PWM channel ensure correct PWM operation even when individual channel settings are changed.

The Timer 1 system is based on a free-running 16-bit counter with a 4-stage programmable prescaler. A timer overflow function allows the software to extend the timing capability of the system beyond the 16-bit range of the counter. Up to four independent Input-Capture functions are used to automatically record the time when a selected transition is detected at a respective timer input pin. Up to five Output-Compare functions are included for generating output signals or for timing software delays. Each of the Input-Capture functions has its own 16-bit time capture latch (Input-Capture register) and each of the Output-Compare functions has its own 16-bit compare register. All timer functions, including the timer overflow, have their own interrupt controls and separate interrupt vectors. Additional control bits permit software to control the edge(s) that trigger each Input-Capture function and the automatic actions that result from Output-Compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is essentially a software-oriented system. This structure is easily adaptable to a very wide range of applications.

The Timer 2 and **Timer 3** systems comprise a prescaler and a 16-bit counter. Each of these modules has three associated 16-bit Output-Compare registers along with a software-programmable Input-Capture or Output-Compare register. Timers also offer an event counting mode of operation, in which the counter is clocked by an external source. Similar to the Timer 1 module, these modules functions, including the timer overflow, have their interrupt controls and separate interrupt vectors and control bits permit software to control the edge(s) that trigger each Input-Capture function and the automatic actions that result from Output-Compare functions.

The Real-Time Interrupt module is used to generate hardware interrupts at a fixed periodic rate. Four different rates are available for the RTI signal. The clock source for the RTI is a free-running timer that cannot be stopped or interrupted, hence RTI timeouts are constants.

The Computer Operating Properly is a simple watchdog module that prevents the whole system from software malfunctions. The COP system can be enabled or disabled by software. It has a configurable clock source that allows scaling watchdog overflow time.

The Pulse Accumulator system is based on an 8-bit counter and can be configured to operate as a simple event counter or for gated time accumulation. Control bits allow the user to configure and control the subsystem operating mode. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The alternate functions of the pulse accumulator input (PAI) pin present some interesting application possibilities.

DESIGN FEATURES:

All DCD's IP Cores are technology independent which means that they are 100% compatible with all FPGA & ASIC vendors e.g.

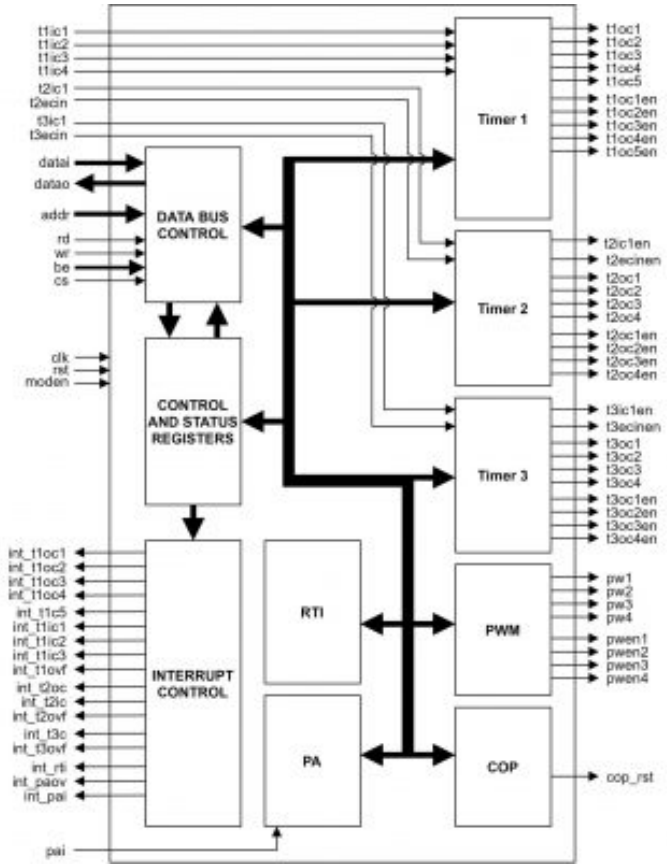
- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- **PWM**:
  - Up to Four 8-bit pulse width or concatenated two

16-bits modulated waveforms
    - Three software-selectable clock sources
    - Software selectable polarity of the output waveform
    - Double buffered period and duty cycle registers for each PWM channel
- **Timer 1**:
    - Free running 16-bit counter with a 4-stage programmable prescaler
    - Timer overflow function
    - Up to four independent, configurable Input Capture functions
    - Up to five Output Compare, configurable functions
    - Interrupt controls and separate interrupt vectors of each IC, OC, and timer overflow
- **Timer 2**:
    - 16-bit counter with a 4-stage programmable prescaler
    - Up to four Output Compare functions
    - One Input Capture function
    - Event counting mode
    - Possibility to stop the counter
    - Timer overflow function
    - Interrupt controls and interrupt vectors of IC, OC, and timer overflow
- **Timer 3**:
    - 16-bit counter with a 3-stage programmable prescaler or with Timer 1 clock rate
    - Up to four Output Compare functions
    - One Input Capture function
    - Event counting mode
    - Possibility to stop the counter
    - Timer overflow function
    - Interrupt controls and interrupt vectors of IC/OC and timer overflow
- **Real-Time Interrupt**:
    - Hardware interrupts at a fixed periodic rate
    - Four different interrupt rates
    - Constant RTI timeouts
- **Computer Operates Properly**:
    - Configurable clock source
    - Scaling of watchdog overflow time
    - Protection from software malfunctions
- **Pulse Accumulator**:
    - 8-bit counter
    - Event counter mode and gated time accumulation mode
    - Maskable interrupts
- Fully synthesizable
- No internal tri-states
- Available system interface wrappers:
    - Native 8-bit interface
    - Native 32-bit interface
    - AMBA – APB / AHB / AXI Lite Bus
- Configurable reset
- Configurable interface control pins activity level
- Simple internal structure configuration

BLOCK DIAGRAM



PERFORMANCE

To provide you with the most accurate and detailed insights about the Lattice performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVEVERABLES

- **Source code:**
    - VERILOG or VHDL Source Code
    - VERILOG or VHDL test bench environment
        - Active-HDL automatic simulation macros
        - ModelSim automatic simulation macros
        - Tests with reference responses
    - Technical documentation
        - Installation notes
        - HDL core specification
        - Datasheet
    - Synthesis scripts
    - Example application
- **Netlist**
    - Netlist for selected FPGA family
    - Sample FPGA project
    - Technical documentation
        - HDL core specification
        - Datasheet
- **Technical support**

- IP Core implementation
- 12 months maintenance
  - Delivery of the IP Core and documentation updates
  - Phone & email support
  - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/