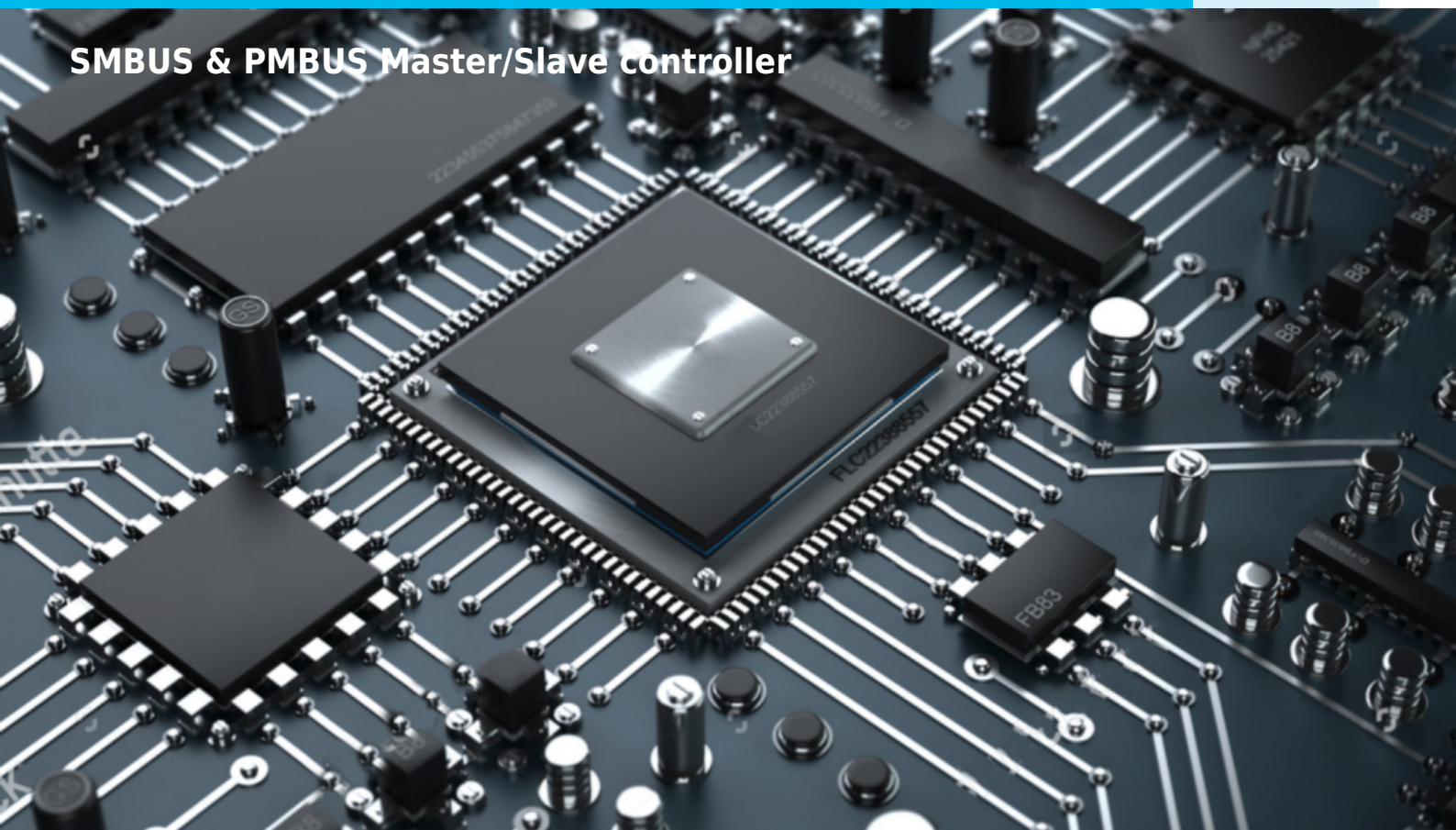
DIGITAL CORE DESIGN

DPSMBUS

SMBUS & PMBUS Master/Slave controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DPSMBUS is a fully-featured module based on the I2C protocol, which supports SMBus and PMBus functionalities.

It can operate as a **DPSMBUSM – Master** and **DPSMBUSS – Slave**. Due to SMBus and PMBus documentation, the module meets the requirements, both for **SMBSDA** and **SMBSCK** acceptable timing intervals.

The DSPMBUS module **supports arbitration and clock synchronization,** which is necessary for multi-master systems. The IP Core, as it's been suggested in the SMBus documentation, has implemented a reaction on a stuck SMBSCK signal in a low state Ttimeoutmin.

DPSMBUS supports transmission speeds up to 3.4 Mb/s, which cover all three acceptable speeds for SMBus and PMBus:

1. 100 kHz,
2. 400 kHz,
3. 1 MHz.

The DPSMBUS in the slave mode has attached internal FIFO, which can store even **up to 256 bytes**. It is also possible to read the status of the transmission including a step where communication failed. Except for SMBSDA and SMBSCK, there is also SMBAlert, which is defined as an interrupt signal between master and slave devices. **Due to the SMBAlert handler, DPSMBUS supports arbitration of slave devices**.

The DPSMBUS in PMBus version accepts **ALERT RESPONSE ADDRESS, GENERAL CALL, DEVICE DEFAULT ADDRESS, ZONE WRITE**, and **ZONE READ** predefined addresses. Also, it is possible to perform group command protocol and even extended command functionality. There are included CONTROL and WRITE PROTECT signals along with their functionality for device supervision.

DESIGN FEATURES:

All DCD's IP Cores are technology independent which means that they are 100% compatible with all FPGA & ASIC vendors e.g.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

- Conforms to v3.1 of the SMBus & 1.3.1 PMBus spec
- Supports all SMBus and PMBus communication sequences
- Performs arbitration and clock synchronization

- **Conforms to v3.1 of the SMBus specification and 1.3.1 PMBus specification**
- Master operation:
  - Master transmitter
  - Master receiver
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports up to 3.4 Mb/s, which covers all acceptable speeds for SMBus and PMBus
- Performs arbitration and clock synchronization
- Multi-master system supported
- Interrupt generation along with SMBAlert bus signal
- Meet the requirements for SMBSDA and SMBCLK acceptable timing intervals
- Allows operation from a wide range of input clock frequencies (built-in 8-bit timer)
- The simple interface allows easy connection to microcontrollers
- User-defined timings
- DSPMBus driver supports all SMBus and PMBus communication sequences
- Fully synthesizable
- Static synchronous design with positive edge clocking and configurable reset
- DSPMBUS driver has implemented CRC8 calculation required for PEC bytes

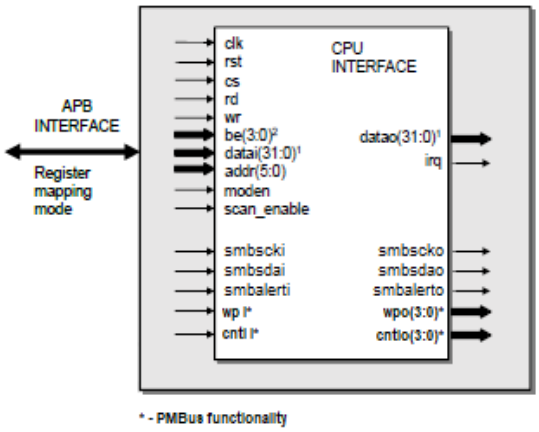
SMBUS

- Compatible with ALERT RESPONSE ADDRESS, and DEVICE DEFAULT ADDRESS predefined addresses
- Implemented FIFO, which can store up to 256 bytes
- Supports SMBAlert arbitration

PMBUS

- Has implemented CONTROL and WRITE PROTECT signals required for PMBus protocol
- Compatible with ALERT RESPONSE ADDRESS, GENERAL CALL, DEVICE DEFAULT ADDRESS, ZONE WRITE, and ZONE READ predefined addresses
- Accepts group command protocol and extended command functionality
- Implemented FIFO, which can store up to 256 bytes

BLOCK DIAGRAM



PERFORMANCE

To provide you with the most accurate and detailed insights about the Lattice performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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