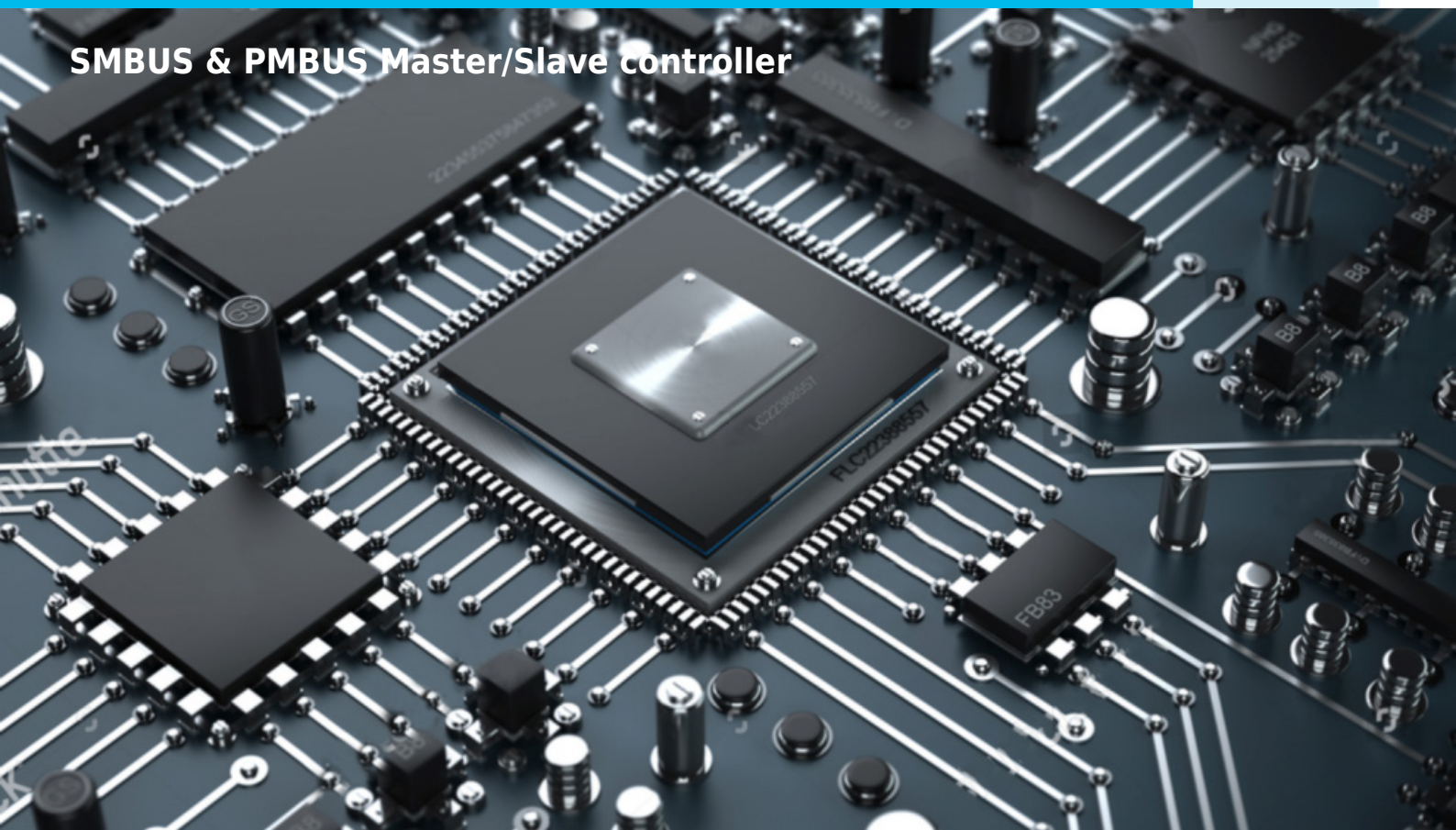
DIGITAL CORE DESIGN

DPSMBUS

SMBUS & PMBUS Master/Slave controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DPSMBUS IP Core — Advanced I²C Module with SMBus and PMBus Support

High-Performance I²C, SMBus & PMBus Communication

The **DPSMBUS IP Core** from DCD-SEMI is a **fully-featured I²C-based module** designed for **embedded systems**, supporting **SMBus** and **PMBus functionalities**. It can operate in both **Master (DPSMBUSM)** and **Slave (DPSMBUSS)** modes, making it versatile for a wide range of **system-on-chip (SoC)**, **FPGA**, and **ASIC designs**.

The DPSMBUS IP Core complies with SMBus and PMBus timing requirements for **SMBSDA** and **SMBSCK** signals, ensuring reliable data communication in **multi-master environments**. Advanced features include **arbitration handling** and **clock synchronization**, with built-in mechanisms to recover from a **stuck SMBSCK line** using minimum timeout detection (**Ttimeoutmin**).

High-Speed Communication

The DPSMBUS supports transmission speeds of up to **3.4 Mb/s**, covering all standard SMBus and PMBus rates:

- **100 kHz** (Standard Mode)
- **400 kHz** (Fast Mode)
- **1 MHz** (Fast Mode Plus)

Advanced Slave Mode Features

In **Slave mode**, DPSMBUS provides an **internal FIFO buffer** capable of storing **up to 256 bytes**, allowing efficient data handling even under high traffic conditions. Key features include:

- Monitoring of **transmission status** and failure points
- **SMBAlert signal** support for interrupt-driven notifications between Master and Slave devices
- Support for **arbitration of multiple Slave devices**

PMBus-Specific Functionality

The PMBus version of DPSMBUS extends capabilities to include:

- **ALERT RESPONSE ADDRESS**, **GENERAL CALL**, **DEVICE DEFAULT ADDRESS**, **ZONE WRITE**, and **ZONE READ**
- **Group command protocol** and **extended command functionality**
- **CONTROL** and **WRITE PROTECT signals** for enhanced device supervision

This ensures seamless integration into **power management systems** and other **complex SMBus/PMBus networks**.

Why Choose DCD-SEMI DPSMBUS IP Core

- Fully compliant with **I²C, SMBus, and PMBus standards**
- Operates as **Master or Slave** with flexible modes
- Supports **100 kHz, 400 kHz, 1 MHz**, up to **3.4 Mb/s** speeds
- **Internal FIFO (256 bytes)** for efficient Slave mode operation
- **SMBAlert handling** for interrupt-driven multi-device arbitration
- **PMBus extended functionality**, group commands, and supervision signals
- Ideal for **embedded systems, SoCs, FPGA, and ASIC applications**

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For technical specifications, integration support, or customization options, contact **info@dcd-semi.com**

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KEY FEATURES

- Conforms to v3.1 of the SMBus & 1.3.1 PMBus spec
- Supports all SMBus and PMBus communication sequences
- Performs arbitration and clock synchronization

DESIGN FEATURES

- **Conforms to v3.1 of the SMBus specification and 1.3.1 PMBus specification**
- Master operation:
  - Master transmitter
  - Master receiver
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports up to 3.4 Mb/s, which covers all acceptable speeds for SMBus and PMBus
- Performs arbitration and clock synchronization
- Multi-master system supported
- Interrupt generation along with SMBAlert bus signal
- Meet the requirements for SMBSDA and SMBCLK acceptable timing intervals
- Allows operation from a wide range of input clock frequencies (built-in 8-bit timer)
- The simple interface allows easy connection to microcontrollers
- User-defined timings
- DSPMBus driver supports all SMBus and PMBus communication sequences
- Fully synthesizable
- Static synchronous design with positive edge clocking and configurable reset
- DSPMBUS driver has implemented CRC8 calculation required for PEC bytes

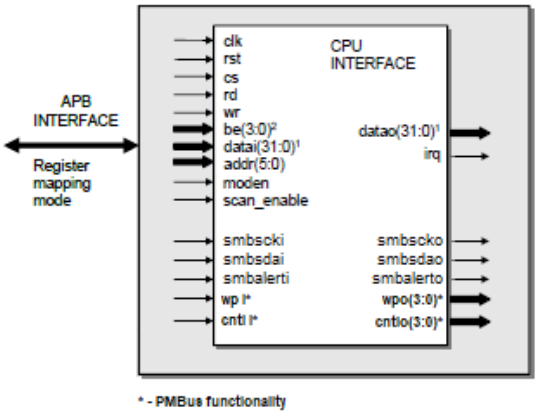
SMBUS

- Compatible with ALERT RESPONSE ADDRESS, and DEVICE DEFAULT ADDRESS predefined addresses
- Implemented FIFO, which can store up to 256 bytes
- Supports SMBAlert arbitration

PMBUS

- Has implemented CONTROL and WRITE PROTECT signals required for PMBus protocol
- Compatible with ALERT RESPONSE ADDRESS, GENERAL CALL, DEVICE DEFAULT ADDRESS, ZONE WRITE, and ZONE READ predefined addresses
- Accepts group command protocol and extended command functionality
- Implemented FIFO, which can store up to 256 bytes

BLOCK DIAGRAM



* - PMBus functionality

PERFORMANCE

For precise LATTICE performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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