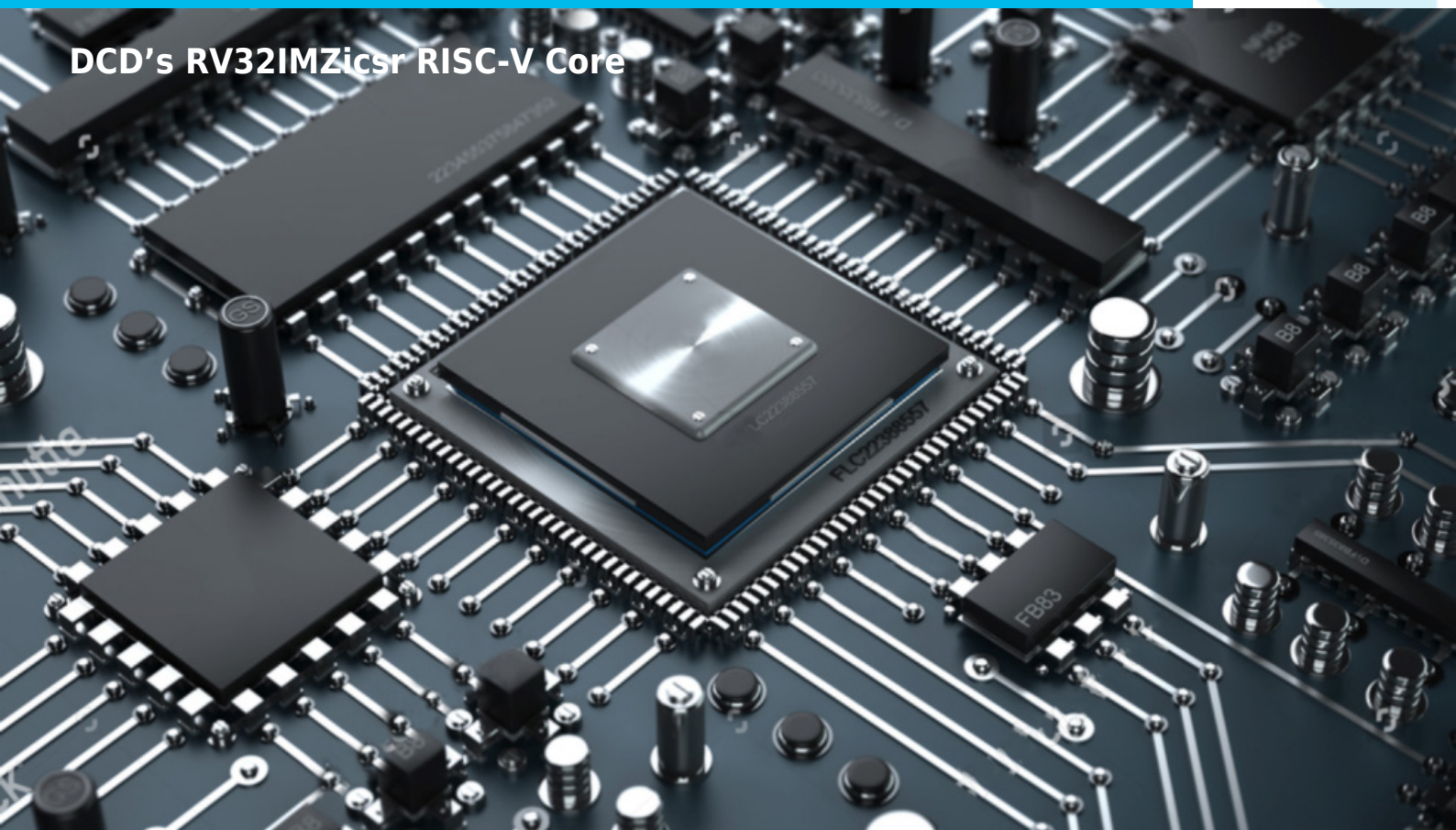
DIGITAL CORE DESIGN

DRV32IMZICSR



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DRV32IMZicsr is a 32-bit RISC-V CPU with **M**, **Zicsr** extensions, and **External Debug support**.

The Core belongs to the latest DCD's DRVX Core Family, with:

- a five-stage pipeline,
- Harvard architecture
- flexible size of program and data memory together with their allocation in address space.

Our solution offers performance tailored to the project requirements, starting from:

- **Dhrystone: up to 1,23 DMIPS/MHz**
- **Coremark: up to 2,45 CoreMark/MHz**

It is possible to select CPU interface as:

- AXI,
- AHB,
- Native.

The DRV32IMZicsr was developed as **ISO26262 Safety Element out of Context (SEooC)** and is technology independent, and compatible with all FPGA and ASIC vendors.

The DRV32IMZicsr can be used along with a wide range of DCD's peripherals, like e.g. **DMA, SPI, UART, PWM, CAN** etc. This holistic approach makes the DRV32IMZicsr core a good choice for application for e.g. Automotive, Internet of Things, Embedded, Consumer Electronics, and more.

The DRV32IMZicsr is a 32-bit core with 32 General Purpose Registers. It performs arithmetic and logic instructions, loads, stores, conditional branches, and unconditional jumps. The proper usage of base instructions provides an additional set of pseudo instructions which are available in the RISC-V assembly language. The **M extension** enables the use of additional integer multiplication and division instructions due to Multiplication and Division unit, which is responsible for handling these instructions. The **Zicsr extension** provides the means to access Control and Status Registers, which in turn enables **interrupt and exception handling** according to version 20211203 of *The RISC-V Instruction Set Manual Volume II: Privileged Architecture*. With Zicsr extension DRV32IMZicsr core is also equipped with performance counters and timers. **External Debug support** utilizes **JTAG debug interface** and is implemented with conformance to the RISC-V Debug Specification 0.13.2 and 1.0.0. That allows core debugging with all the tools compatible with this specification available on the market.

The DRV32IMZicsr core is delivered with a fully automated test bench and a complete set of tests, allowing easy package validation at each stage of the SoC design flow.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Five-stage pipeline
- Harvard architecture
- RV32I Base RISC-V ISA
- M extension
- Zicsr extension
- External Debug support
- JTAG debug interface
- Conformance to the RISC-V Debug Specification 0.13.2 and 1.0.0
- Highly configurable, including:
  - Flexible memory size and allocation
  - Interface selection: AXI, AHB, Native
- M privilege level support
- Interrupt and exception handling
- Performance counters and timer
- Wide range of supported peripherals, including:
  - DMA
  - SPI
  - UART
  - PWM
  - and more
- Developed as ISO26262 Safety Element out of Context (SEooC)
- Technology-independent HDL Source Code
- **Performance:**
  - **Dhrystone: up to 1,23 DMIPS/MHz**
  - **Coremark: up to 2,45 CoreMark/MHz**

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS – ask for more at info@dcd.pl

PERFORMANCE

Our solution offers performance tailored to the project requirements, starting from:

- **Dhrystone: up to 1,23 DMIPS/MHz**
- **Coremark: up to 2,45 CoreMark/MHz**

To provide you with the most accurate and detailed insights about Xilinx performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVERABLES

- Source code:
  - VHDL Source Code
- VHDL test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - VCS automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation
- 12 months maintenance
  - Delivery of the IP Core and documentation updates
  - Phone & email support
  - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/