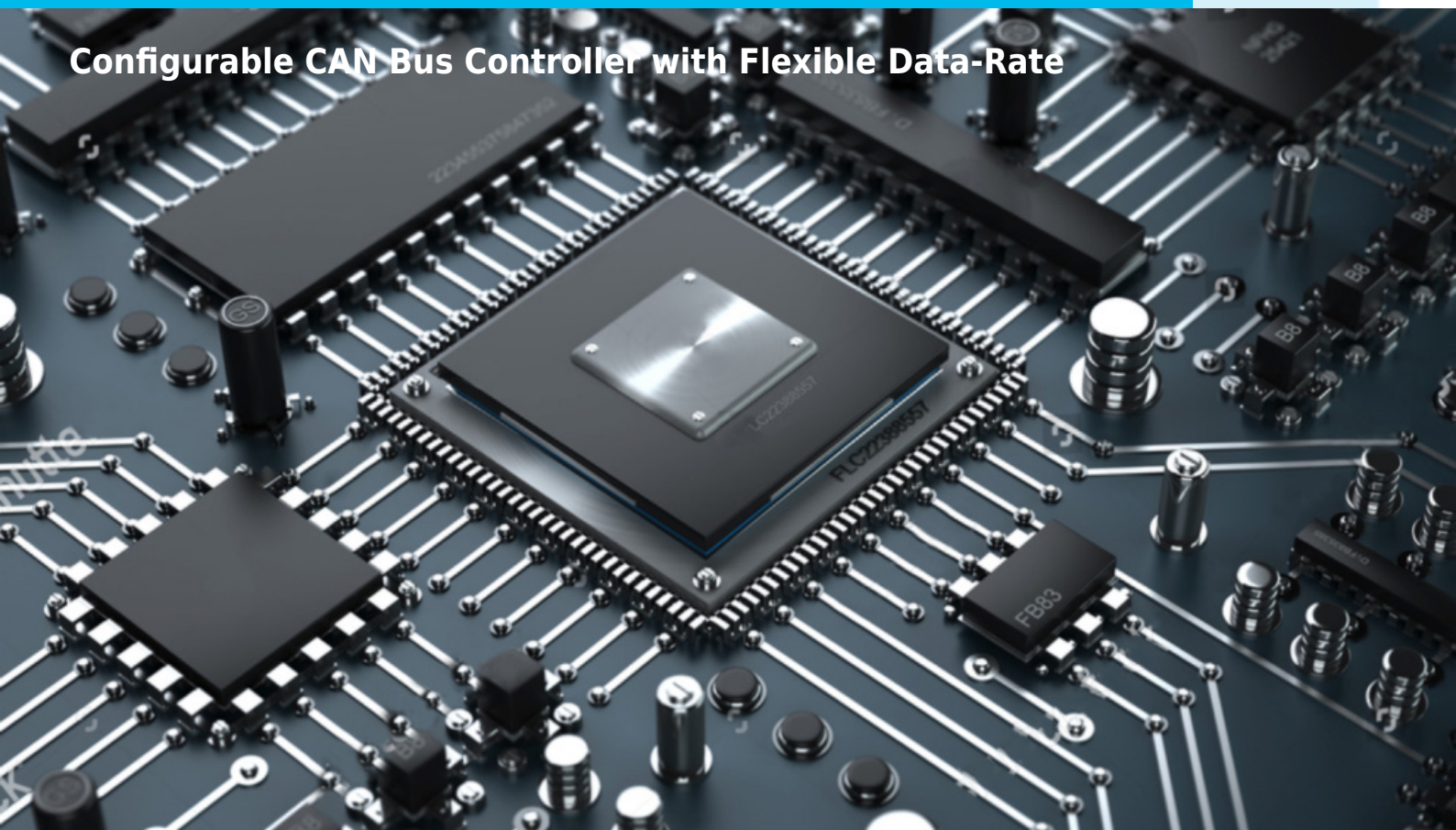
DIGITAL CORE DESIGN

# CAN FD



## COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

## IP CORE OVERVIEW

Introducing DCD's Ingenious CAN FD IP Core: Empowering Engineers with Unparalleled Flexibility.

When it comes to seamlessly infusing cutting-edge Controller Area Network (CAN) capabilities into diverse systems, look no further than DCD's CAN FD IP Core. This engineering marvel can be harnessed as a standalone powerhouse, an integral part of an ASIC, or an FPGA marvel. Guided by the ISO11898-1:2015 standard, it ushers in flawless communication aligned with industry-favorite protocols, making it a game-changer for engineers and innovators.

Engineered to cater to both Classical CAN and the dynamic CAN FD, this module does require external transceiver hardware to establish a tangible link to the CAN bus. Our ingenious approach employs a single or dual-ported Message RAM, strategically situated outside the module, connected through the versatile Generic Master Interface. This meticulous design simplifies the art of message handling, ensuring efficiency at every turn.

The pièce de résistance? Seamlessly uniting the host CPU with the CAN IP Core module via the 32-bit Generic Interface. This harmonious partnership guarantees a frictionless fusion, orchestrating a symphony of data exchange. But we don't stop there. Compatibility is our middle name, as our Core seamlessly supports a roster of interface wrappers including, but not limited to:

- **AMBA – APB / AHB / AXI Lite Bus**
- **Altera Avalon Bus**
- **Xilinx OPB Bus**

Variety is the spice of engineering life, and that's why our IP core shines in two tantalizing flavors: the dynamic Basic and the robust Safety-Enhanced.

Prepare to be awestruck – our ingenious creation is not just an IP core; it's a safety-critical masterpiece designed as an ISO26262-10 Safety Element out of Context. As if that's not impressive enough, it can be amped up with vital safety mechanisms, complete with comprehensive ISO26262 soft IP SEooC work products. Expect nothing less than a complete Failure Modes Effects and Detection Analysis (FMEDA) – a guidebook that unravels seamless IP integration into your unique system, and a roadmap to conduct meticulous system-level safety analysis.

As for the skeptics, rest assured. We've subjected our safety-related work products to a third-party, independent audit, elevating our masterpiece's trustworthiness.

Safety metrics? Oh, they are more than met. Both IPs boast an Automotive Safety Integrity Level (ASIL-B), with the Single Point Fault Metric (SPFM) soaring past 90% and the Latent Fault Metric (LFM) comfortably exceeding 60%. In simple terms – they're bulletproof.

But wait, there's more. Our ASIL-B ready design seamlessly slides into Automotive Safety Systems at the ASIL-B level, but here's the kicker: we've got higher ASIL-level ready IP in our arsenal, if you dare to dream bigger.

Curiosity piqued? Dive into this engineering marvel by reaching out to our support team. Let the innovation begin!

***CAN FuSa white papers***

**DESIGN FEATURES:**

***ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.***

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

## KEY FEATURES

- Designed in accordance to **ISO 11898-1:2015**
- Supports **CAN 2.0B** and **CAN FD** frames
- Support up to 64 bytes data frames
- **Flexible data-rates supported**
- Supports emotas CANopen FD stack
- 8/16/32-bit CPU slave interface with small or big endianness
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames
- **Data rate up to 8 Mbps**
- Up to 32 Hardware message filtering (dual/single filter)
- Configurable size of RX/TX memory
- Overload frame is generated on FIFO overflow
- **Normal & Listen Only Mode**
- Transceiver Delay Compensation up to three data bit long
- Single Shot transmission
- Ability to abort transmission
- Readable error counters
- **Last Error Code**
- Fully synthesizable

- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready
- **Available system interface wrappers:**
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Lite Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

## UNITS SUMMARY

**Interface Management Logic (IML)** – interprets commands from the CPU, provides interrupt and status indication.
**Bit Stream Processor (BSP)** – translates messages into frames and vice versa.
**Baud Rate Prescaler (BRP)** – defines the length of time quantum.
**Bit Timing Logic (BTL)** – processes the bit time, calculates position of the sample point and performs synchronization.
**Error Management Logic (EML)** – is responsible for fault confinement handling.
**Acceptance Filter (ACF)** – decides, whether incoming messages are accepted or not, based on filter registers settings.
**TX/RX RAM interfaces** – interfaces to external dual port memories used by the DCAN core, to store received and transmitted frames.

## PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** Devices (all key features included). Core performance in ASIC devices – Flexible Datarate functionality is **OFF**):

| Technology /optimization | Speed grade | Area [gates] | $F_{max}$ |
|---|---|---|---|
| 0.18u area | typical | 5 800 | 100 MHz |
| 0.18u speed | typical | 6 300 | 300 MHz |
| 0.09u area | typical | 5 200 | 200 MHz |
| 0.09u speed | typical | 6 700 | 400 MHz |

The following table gives a survey about the Core area and performance in **ASIC** Devices (all key features included). Core performance in ASIC devices – Flexible Datarate functionality is **ON**):

| Technology /optimization | Speed grade | Area [gates] | $F_{max}$ |
|---|---|---|---|
| 0.18u area | typical | 11 900 | 100 MHz |
| 0.18u speed | typical | 12 500 | 300 MHz |
| 0.09u area | typical | 11 500 | 200 MHz |
| 0.09u speed | typical | 12 900 | 400 MHz |

## DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

## APPLICATIONS

- Automotive, industrial
- Embedded communication systems

## LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
***– Single-Site license option*** – dedicated to small and middle sized companies which run their business at one place.
***– Multi-Site license option*** – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

## CONTACT

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