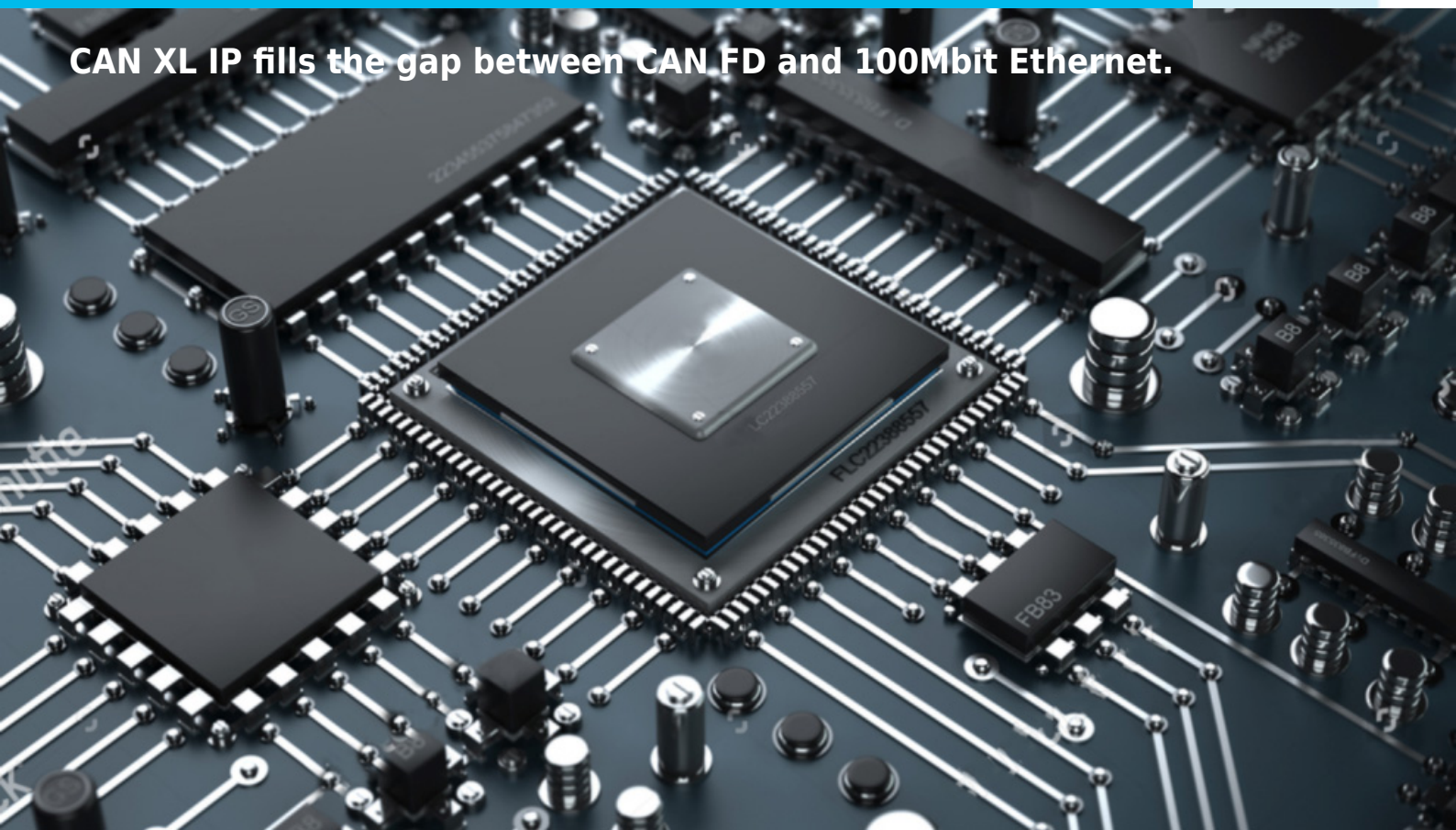
DIGITAL CORE DESIGN

DCAN XL



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DCAN XL IP CORE — NEXT-GENERATION CAN XL CONTROLLER BRIDGING CAN FD AND 100 MBIT ETHERNET

The **DCAN XL IP Core** from DCD-SEMI represents a major leap forward in in-vehicle communication, bridging the gap between **CAN FD** and **100 Mbit Ethernet**. Designed for high-bandwidth, next-generation automotive architectures, it supports data rates up to **20 Mbit/s** and payloads up to **2048 bytes**, enabling dramatically faster and more flexible data transmission than previous CAN standards.

65kBWith support for **higher-layer protocols**, **Ethernet frame tunneling**, and extended data fields, the DCAN XL IP Core delivers the scalability required for emerging automotive, industrial, and smart mobility applications.

BACKWARD-COMPATIBLE WITH CAN, CAN FD, AND CAN XL

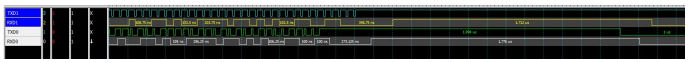
While offering advanced capabilities, the DCAN XL IP Core retains the proven benefits of the CAN ecosystem. It provides full backward compatibility with:

- **Classical CAN**
- **CAN FD**
- **CAN XL**

Physical connection to the CAN bus requires external transceivers, with:

- Standard CAN transceivers recommended below **10 Mbit/s**
- **CAN SIC XL** transceivers required above **10 Mbit/s**

This ensures reliable communication tailored to system requirements.



OPTIMIZED ARCHITECTURE FOR HIGH-SPEED MESSAGE HANDLING

The DCAN XL IP Core utilizes an external **single- or dual-ported Message RAM**, connected through a **Generic Master Interface** for optimal throughput. This design enables:

- High-speed message processing
- Reduced CPU load
- Scalable RAM configuration
- Flexible system integration

The host CPU connects through a **32-bit Generic Interface**, compatible with widely used SoC/FPGA bus wrappers such as:

- **AMBA**
- **Intel/Altera Avalon Bus**
- **Xilinx OPB Bus**

AVAILABLE IN BASIC AND SAFETY-ENHANCED (ISO 26262 SEOOC) VERSIONS

The DCAN XL IP Core is offered in:

- **Basic Version**
- **Safety-Enhanced Version**, designed as an **ISO 26262-10 Safety Element out of Context (SEooC)**

The Safety-Enhanced variant provides:

- Complete **ISO 26262 safety documentation**
- Fully validated **FMEDA analysis**

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- Optional integrated safety mechanisms
- Third-party audited work products

ASIL-B READY FUNCTIONAL SAFETY — EXTENSIBLE TOWARD ASIL-D

The completed safety analysis confirms that the **DCAN FD FULL** IP Core meets all **ASIL-B** functional safety requirements, achieving the following key metrics:

- **SPFM > 90%** (Single Point Fault Metric)
- **LFM > 60%** (Latent Fault Metric)

These results validate the suitability of the DCAN FD FULL for integration into automotive systems targeting **ASIL-B** safety goals.
Additionally, **DCD-SEMI can provide enhanced variants** tailored to support architectures requiring higher safety integrity levels — **including ASIL-D** — to meet specific OEM or Tier-1 requirements.

WHY ENGINEERS CHOOSE DCAN XL

- Supports CAN, CAN FD, and CAN XL
- Up to 20 Mbit/s and 2048-byte payloads
- Ethernet tunneling & higher-layer protocol support
- CPU-friendly architecture
- ASIC/SoC/FPGA-ready design
- Developed in line with ISO26262 as SEooC.
- ASIL-B & ASIL-D compliant.
- Delivered with functional safety-related documentation.
- Independent third-party audit assessment.

DCD-SEMI automotive IP Cores

	DCAN	DCAN-FD	DCAN-FD Full	DCAN-XL	DLIN	DSENT	DPSI5
Supported protocol	CAN	CAN-FD	CAN-FD	CAN-XL	LIN	SENT	PSI5
Data rate up to	1Mbps	8Mbps	8Mbps	20Mbps	20kbps	30kbps	189kbps
Cost vs complexity	middle	middle	middle high	high	low	low	middle
Best for	Vehicle networks and industrial automation	High speed communication	DCAN FD + multiple TX/RX buffers/FIFOs, timestamps, advanced message filtering	High-performance automotive	Low-cost automotive nodes	Sensor → ECU timing-based data	Safety sensors (airbag, ABS)
ISO26262 Functional Safety	yes	yes	yes	yes	yes	yes	yes

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For additional technical details or optional features, contact **info@dcd-semi.com**

KEY FEATURES

- Designed in accordance with **ISO 11898-1:2024** specification and **CiA610-1 specification**
- **Supports CAN, CAN FD and CAN-XL frames**
- Supports up to 64 bytes CAN FD frame and up to 2048 bytes CAN-XL data frame
- Flexible data rates supported
- **AUTOSAR support**
- **SAE J1939 support**
- Simple 8/16/32-bit CPU slave interface
- **Data rate up to 1Mbps in Classic CAN mode, up to 8Mbps in FD mode, up to 20Mbps in XL mode**
- Optional PWM coding allows bit-rates of 10 Mbit/s and more depending on the physical network design
- Up to 128 Base ID filters
- Up to 64 Extended ID filters
- 2 Configurable receive FIFO
- Overload frame is generated on FIFO overflow
- Up to 32 dedicated Transmit Buffers
- Configurable Transit Buffers to FIFO or QUEUE
- Configurable Transmit Event FIFO
- Normal and Listen Only modes supported
- Transmitter Delay Compensation up to six data bits long
- Ability to abort transmission
- Readable error counters
- Last Error Code
- Timestamp according to CiA 603 support
- Two configurable interrupt lines
- Two clock domains (CAN clock and CPU clock)
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

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UNITS SUMMARY

Interface Management Logic (IML) – interprets commands from the CPU, provides interrupt and status indication.
Bit Stream Processor (BSP) – translates messages into frames and vice versa.
Baud Rate Prescaler (BRP) – defines the length of time quantum.
Bit Timing Logic (BTL) – processes the bit time, calculates position of the sample point and performs synchronization.
Error Management Logic (EML) – is responsible for fault confinement handling.
Acceptance Filter (ACF) – decides, whether incoming messages are accepted or not, based on filter registers settings.
TX/RX RAM interfaces – interfaces to external dual port memories used by the DCAN core, to store received and transmitted frames.

TYP => 65 kB (2 RX FIFO with 8 elements, 8 RX BUFFERS, 8 TX BUFFERS, 8 deep TX EVENT FIFO, 56 filters)
MIN => 14kB (1 RX FIFO with 4 elements, No RX BUFFERS, 3 TX BUFFERS, 3 deep TX EVENT FIFO, 48 filters)

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** Devices.

Technology	FuSa	Cell Area Gate eq.
90nm	yes	37300
90nm	no	35000
110nm	yes	37300
110nm	no	35000

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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