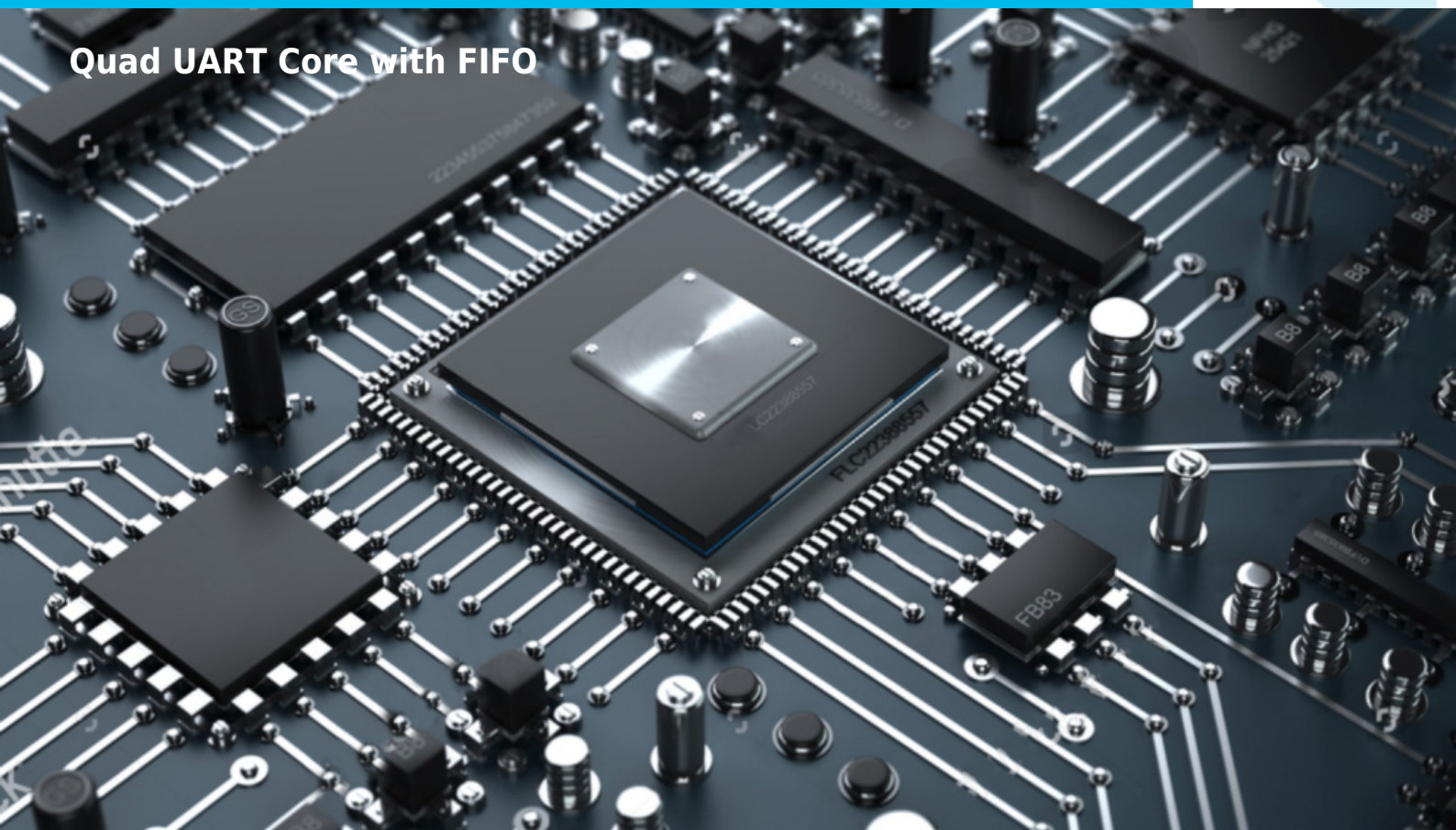
DIGITAL CORE DESIGN

D2694

Quad UART Core with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D2694 Quad UART IP Core – High-Performance Multi-Channel UART for FPGA & ASIC

The **D2694** from **DCD-SEMI** is a **Quad-channel Universal Asynchronous Receiver/Transmitter (UART)** soft core, **software-compatible with SC2694**, designed for seamless integration into **APB, AHB, and AXI bus architectures**. This high-performance core is ideal for **multi-UART embedded systems, terminal clusters, and communication-intensive FPGA/ASIC designs**.

Four Full-Duplex UART Channels

The D2694 provides:

- **Four independent full-duplex UART channels** in a single core
- **8-character receive and transmit FIFOs** per channel for efficient buffering
- **Watchdog timers** for each receiver channel to ensure reliable data reception
- **Mode register configuration and extended baud rate support** for each channel

This allows engineers to implement **high-throughput, low-latency serial communication** in complex multi-channel systems.

Flexible Baud Rate & Clocking

Each UART channel supports **independent operating speeds**, configurable via:

- **27 fixed baud rates**
- **16× clock derived from a programmable counter/timer**
- **External 1× or 16× clock input**

This flexible clocking mechanism enables **dual-speed channel applications**, making the D2694 ideal for **clustered terminal systems, industrial communication, and multi-UART interfaces**.

Programmable Interrupts and Modem/DMA Support

- **Independent transmitter and receiver interrupts** programmable to application requirements
- Supports **polled or interrupt-driven operation**
- Integrated **modem interface** and **DMA capability**
- Reduces CPU load while ensuring **robust and reliable data handling**

Key Features

- Quad-channel **UART core compatible with SC2694**
- Independent **baud rate and mode configuration per channel**
- **8-character FIFO** for transmit and receive paths
- **Watchdog timers** for data reliability
- Supports **modem control and DMA interface**
- Compatible with **APB, AHB, and AXI bus architectures**
- Fully **technology-independent** for FPGA or ASIC implementation

Ideal Applications

- High-throughput **multi-UART embedded systems**
- Terminal clusters and industrial serial communication networks
- Multi-channel **FPGA/ASIC UART integration**

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- Legacy SC2694 replacement or upgrade solutions

Verification-Ready and Technology Independent

Like all DCD-SEMI UART cores, **D2694** comes with:

- **Fully automated testbench**
- **Comprehensive validation suite** for SoC integration
- Technology-independent design for **implementation across FPGA and ASIC processes**

Feature / IP Core	D2692	D2694	D2698
Core Type	Dual UART (DUART)	Quad UART (QUART)	Octal UART (OUART)
Channels	2 full-duplex	4 full-duplex	8 full-duplex
FIFO Size	8-character RX/TX	8-character RX/TX	8-character RX/TX
Watchdog Timer	Yes, per receiver	Yes, per receiver	Yes, per receiver
Mode Register 0	Yes	Yes	Yes
Extended Baud Rate	Yes	Yes	Yes
Programmable Interrupts	Receiver & transmitter	Receiver & transmitter	Receiver & transmitter
Modem Interface	Yes	Yes	Yes
DMA Support	Yes	Yes	Yes
Independent Channel Speed	Yes	Yes	Yes
Clocking Options	Fixed, 16× derived, external	Fixed, 16× derived, external	Fixed, 16× derived, external
Polled / Interrupt Operation	Supported	Supported	Supported
Software Compatibility	SC26C92, SCC2692, SCN2681	SC2694	SC2698
Key Applications	Dual-speed terminals, embedded systems	Multi-UART clusters, industrial systems	High-density multi-UART systems, telecom, gateways
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes

Notes:

- **D2692:** Dual-channel UART for simpler embedded applications or legacy SC26C92 replacement.
- **D2694:** Quad-channel UART suitable for clustered terminals or medium multi-UART systems.
- **D2698:** Octal UART designed for high-density, high-throughput serial communication applications.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

Feature / IP Core	D16450	D16550	D16750	D16752	D16950	D8530	DMESCC	D26C92	DµART	D2692	D2694	D2698
Core Type	Classic UART	FIFO-based UART	High-performance UART	Dual-channel high-performance UART	High-throughput UART	Dual-channel USART	Dual-channel multiprotocol serial controller	Dual-channel UART / DUART	Lightweight soft UART	Dual UART (DUART)	Quad UART (QUART)	Octal UART (OUART)
Channels	1	1	1	2	1	2	2	2	1	2	4	8
UART Compatibility	16450 / TL16C450	16550 / TL16C550A	16750 / TL16C750	16752 / TL16C752	16450–16750 + OX16C950	Zilog 8530-compatible	Enhanced ESCC-compatible	SC26C92 / SCC2692 / SCN2681 compatible	Generic soft UART	SC26C92 / SCC2692 compatible	SC2694	SC2698
Supported Modes	Asynchronous	Asynchronous & FIFO	Asynchronous & FIFO	Asynchronous & FIFO, dual-channel	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & FIFO	Asynchronous	Asynchronous & FIFO	Asynchronous & FIFO	Asynchronous & FIFO
FIFO Support	☐ No FIFO	☐ 16-byte FIFO	☐ 512-byte FIFO	☐ 64-byte FIFO per channel	☐ 128-byte FIFO	Optional / limited	Optional / configurable	☐ 8-character RX/TX FIFO per channel	☐ No FIFO	☐ 8-character RX/TX FIFO	☐ 8-character RX/TX FIFO	☐ 8-character RX/TX FIFO
FIFO Trigger Levels	—	Configurable	Programmable (1–512)	Programmable per channel	Programmable (1–127)	—	—	Programmable per channel	—	Programmable per channel	Programmable per channel	Programmable per channel
CPU Load	High	Medium	Low	Low	Low	Medium	Medium	Medium	Low	Medium	Medium	Medium
Error Reporting	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break, idle	Parity, framing, overrun, break	Parity, CRC, abort	Parity, CRC, abort	Parity, framing, overrun, break	Overrun, framing	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break
CRC Generation / Check	No	No	No	No	No	Yes (sync modes)	Yes (sync modes)	No	No	No	No	No
Modem Control	Full	Full	Advanced autoflow	Hardware/software flow control, TCR	Advanced autoflow	Yes (both channels)	Yes (both channels)	Yes, DMA & modem interface	Optional via software	Yes	Yes	Yes
Interrupt System	Programmable	Programmable	Advanced programmable	Programmable, FIFO RDY register	Advanced programmable	Programmable	Programmable	Programmable, independent per channel	Lightweight programmable	Programmable	Programmable	Programmable
DMA Support	Interrupt-optimized	Interrupt-optimized	Yes	Yes	Yes	Yes	Yes	Yes	Optional	Yes	Yes	Yes
Clocking Options	Internal BRG	Internal BRG	Internal / external	Internal / external	Internal / external	Internal BRG	Internal BRG	Independent programmable clock, external or 16× derived	Internal / external programmable	Fixed, 16× derived, external	Fixed, 16× derived, external	Fixed, 16× derived, external
Special Features	Legacy compatibility	Configurable FIFO & Modem	Deep FIFO (512B), autoflow, 16450 modes	Dual-channel, FIFO RDY register, hardware/software flow control, TCR	Deep FIFO, 9-bit mode, synchronous	Legacy protocol support (HDLC, SDLC)	Enhanced block transfer, vectored interrupts	Independent channel baud rates, watchdog timers, dual-speed operation	Lightweight, flexible baud rate, minimal CPU load, standalone or integrated use	Dual-channel independent speed, watchdog timers	Quad-channel, independent baud rates, multi-UART cluster support	Octal-channel, independent baud rates, high-density multi-UART system
Typical Applications	Legacy UART replacement	FIFO-based legacy upgrade	High-throughput UART, legacy replacement	Dual-channel embedded UART-TL16C752 replacement	Telecom, industrial gateways	Telecom, LAN, industrial serial	Communications controllers, protocol engines	Dual-speed terminals, embedded dual UART systems	Embedded soft UART, low-resource FPGA/ASIC designs	Dual-speed terminals, embedded dual UART systems	Multi-UART clusters, industrial systems	High-density multi-UART systems, telecom, gateways
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

KEY FEATURES

- Software compatible with SC28C94 UARTs
- Configuration capability
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character FIFOs for each receiver and transmitter
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 27 fixed rates: 50 to 230.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode:
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port:
  - Can serve as clock, modem, or control inputs

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- Change of state detection on four inputs
- Multi-function 8-bit output port:
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
  - FIFO states for DMA and modem interface
- Versatile interrupt system:
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates: 1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- Power down mode
- Receiver timeout mode

UNITS SUMMARY

Data Bus Buffer – The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block, to allow read and write operations, to take place between the controlling CPU and the QUART.

Operation Control – The operation control logic receives operation commands from the CPU and generates appropriate signals, to internal sections, to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus.

Interrupt Control – A single active-Low interrupt output (INTR) is provided, which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTR to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration. These pins may be used for DMA and modem control.

BRG – Baud Rate Generator – The baud rate generator operates from the oscillator or external clock input and is capable of generating 27 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a “1” gives additional baud rates to 230.4kB. These will be in the 16X mode. All the baudrates are calculated for the external clock: 3.6864MHz. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

Counter-Timer – The Counter/Timer is a programmable 16–bit divider that is used for generating miscellaneous clocks or generating timeout periods. These clocks may be used by any or all of the receivers and transmitters in the QUART or may be directed to an I/O pin for miscellaneous use.

Input/Output Port – The D2694 has four I/O lines for each channel. Each line can be individually programmed as input or output line using respective bit location of I/O Control register. The 16 I/O ports are accessed and/or controlled by five (5) registers: IPR, ACR, I/OPCR, IPCR, OPR. Each UART has four pins. Two of these pins have Change of State Detectors (COS). These detectors set whenever the pin to which they are attached changes state. (1 to 0 or 0 to 1) The ªChange of State Detectorsº are enabled via the ACR. When enabled the COS devices may generate interrupts via the IMR and IPCR registers. Note that when the COS interrupt is enabled that any one or more of the four COS bits in the IPCR will enable the COS bidding. Each of the channel’s four I/O lines are configured as inputs on reset.

PROGRAMMING

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in
Table 1. The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example,
changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and
transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped. Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register “Miscellaneous Commands”. Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software. Mode,
command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H‘02’ and H‘0A’ should never be read during normal operation since they are reserved for internal diagnostics.

APPLICATIONS

- Serial Data communication applications
- Modem interface

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- Embedded microprocessor boards

PERFORMANCE

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DELIVERABLES

- HDL Source Code
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  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

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Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

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The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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