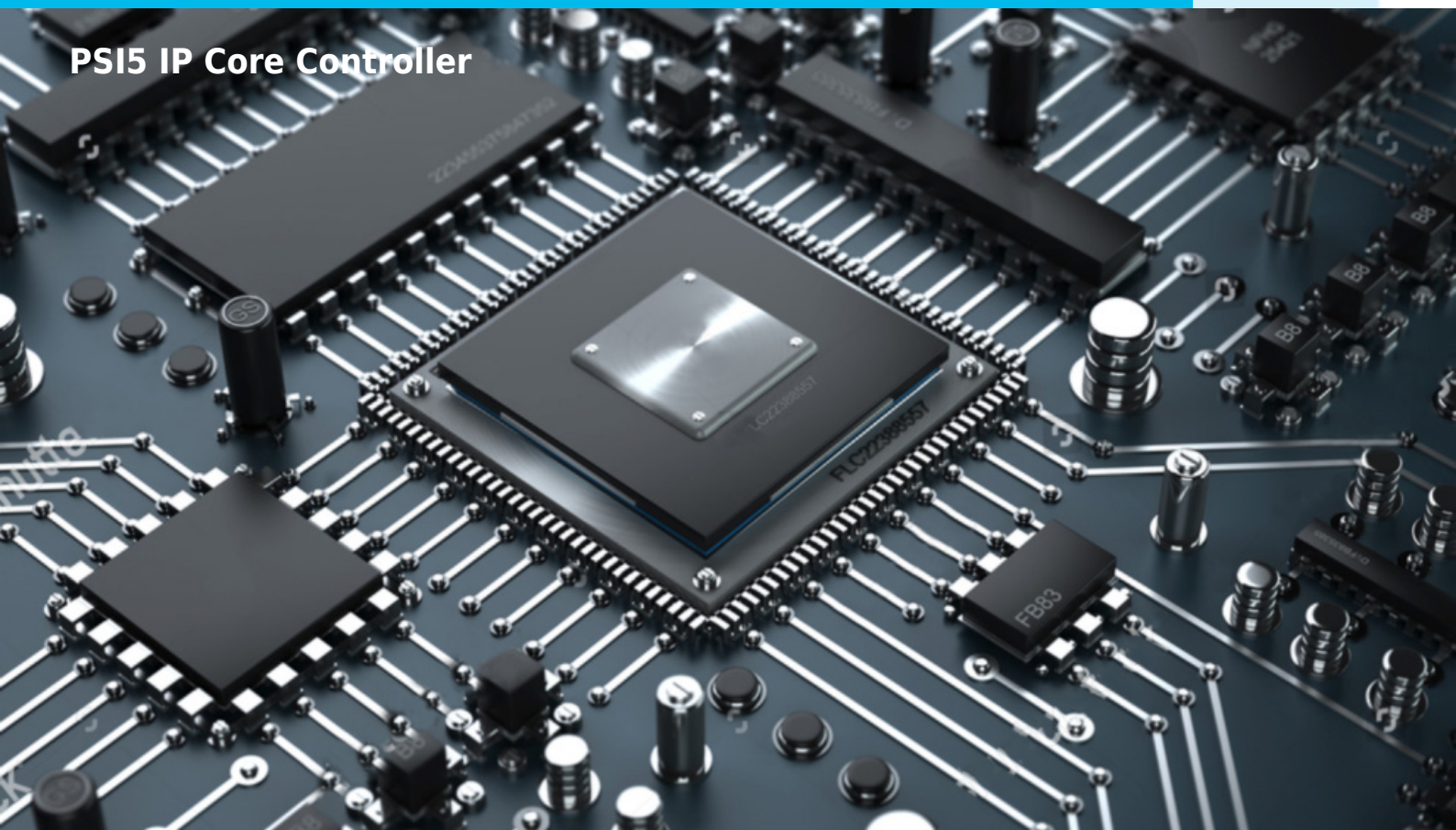
DIGITAL CORE DESIGN

DPSI5

PSI5 IP Core Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DPSI5 IP CORE — HIGH-RELIABILITY PSI5 CONTROLLER FOR AUTOMOTIVE SENSORS

ADVANCED PERIPHERAL SENSOR INTERFACE (PSI5) FOR ECUS

The **DPSI5 IP Core** from DCD-SEMI is a hardware implementation of the **Peripheral Sensor Interface (PSI5) protocol**, fully compliant with **PSI5 specification V2.3**. Designed for integration into **Electronic Control Units (ECUs)**, DPSI5 enables reliable communication with up to **six automotive sensors** per bus, supporting advanced applications from **airbags** to **vehicle dynamics and pedal angle sensors**.

Data transmission from sensors to the ECU uses **current modulation** on the power supply line at **125 kbit/s** or **189 kbit/s**, decoded via **Manchester coding**. Transmission from the ECU to sensors is achieved through **voltage modulation**, ensuring robust, low-latency communication.

DPSI5 supports both **asynchronous and synchronous**

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operation, with flexible data word lengths ranging from **8 to 28 bits**, and ensures message integrity via **CRC checks or bit parity**.

KEY FEATURES OF DPSI5 IP CORE

- **Two-Wire Current Interface:** Simplified wiring for power and data reduces system cost and complexity
- **Manchester-Coded Digital Data Transmission:** Ensures synchronization, robustness, and EMI resilience
- **High-Speed Data Transmission:** Supports 125 kbps, with optional 189 kbps mode for higher-performance sensors
- **High Electromagnetic Compatibility (EMC):** Low-impedance design provides excellent resistance to EMI
- **Flexible Data Frames:** Supports variable data word lengths (8–28 bits) for diverse sensor requirements
- **Asynchronous & Synchronous Modes:** ECU-controlled or sensor-initiated communication
- **Multi-Sensor Bus Configurations:** Up to six sensors per PSI5 bus, supporting both point-to-point and bus setups

ADVANTAGES OF PSI5

- **Cost Efficiency:** Minimal cabling and connectors reduce overall system costs
- **High Reliability:** Proven for critical applications like airbags, accelerator pedals, and acceleration sensors
- **Flexibility:** Adaptable for various sensor types and automotive applications

Integrating the **DPSI5 IP Core** allows manufacturers to build **highly reliable, cost-effective automotive sensor systems** while maintaining **robust performance** in harsh environments.

SAFETY-ENHANCED DESIGN WITH ISO 26262 COMPLIANCE

The DPSI5 IP Core is available in:

- **Basic Version** — for standard automotive sensor communication
- **Safety-Enhanced Version** — developed as an **ISO26262-10 Safety Element out of Context (SEooC)**

The Safety-Enhanced variant includes optional **functional safety mechanisms**, **complete FMEDA analysis**, and step-by-step **integration guidance** to support system-level safety analysis. All work products have undergone **third-party independent audits**, ensuring reliability and compliance.

ASIL-B READY FOR AUTOMOTIVE SAFETY SYSTEMS

Safety metrics demonstrate compliance with **ASIL-B**:

- **SPFM > 90%** (Single Point Fault Metric)
- **LFM > 60%** (Latent Fault Metric)

The DPSI5 IP Core is ready for integration into **ASIL-B automotive systems**, with optional availability for **higher ASIL-level designs** upon request.

WHY CHOOSE DCD-SEMI DPSI5 IP CORE

- PSI5 V2.3 compliant for automotive sensors
- Supports **125 kbps and 189 kbps** data rates
- Up to **six sensors per bus**
- Flexible **8–28 bit data frames**, asynchronous/synchronous operation
- High EMC robustness and reliability
- **FPGA & ASIC ready**
- Safety-Enhanced version with **ISO26262 SEooC compliance**
- **ASIL-B ready**, with optional higher ASIL-level support

DPSI5, LIKE ALL DCD'S IP CORES, IS TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For technical specifications, integration support, or safety-enhanced options, contact **info@dcd-semi.com**

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DCD-SEMI automotive IP Cores

	DCAN	DCAN-FD	DCAN-FD Full	DCAN-XL	DLIN	DSENT	DPSI5
Supported protocol	CAN	CAN-FD	CAN-FD	CAN-XL	LIN	SENT	PSI5
Data rate up to	1Mbps	8Mbps	8Mbps	20Mbps	20kbps	30kbps	189kbps
Cost vs complexity	middle	middle	middle high	high	low	low	middle
Best for	Vehicle networks and industrial automation	High speed communication	DCAN FD + multiple TX/RX buffers/FIFOs, timestamps, advanced message filtering	High-performance automotive	Low-cost automotive nodes	Sensor→ECU timing-based data	Safety sensors (airbag, ABS)
ISO26262 Functional Safety	yes	yes	yes	yes	yes	yes	yes

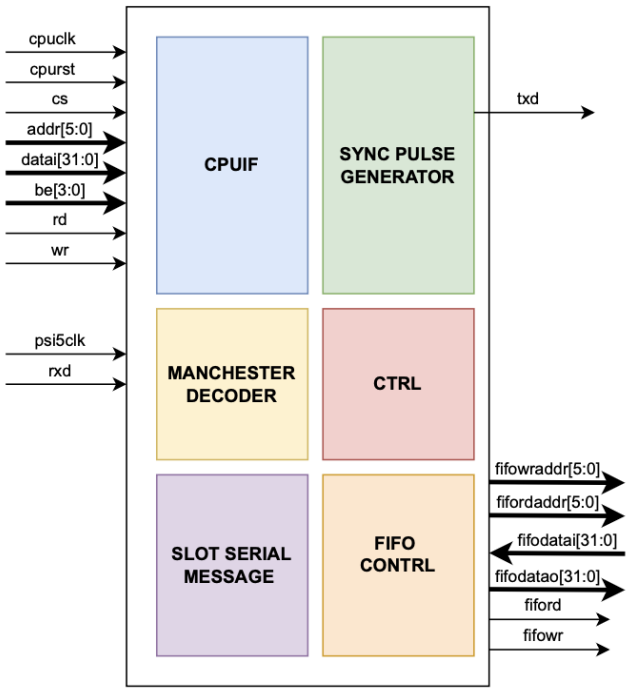
KEY FEATURES

- Supports bidirectional communication between ECU-to-sensor
- Asynchronous or synchronous operation
- Manchester decoder digital data transmission
- Data transmission speed 125Kbit/s or 189 Kbit/s
- Support up to 6 time slots between SYNC pulses
- Configurable data word length from 8 to 28 bits
- Configurable type of frame checking each slot
- CRC or parity checking
- 24 bits time stamp
- Configurable RX FIFO
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- Scan test ready

APPLICATIONS

- **Airbag Systems**
- **Chassis & Powertrain Monitoring**
- **Industrial Automation**

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** Devices (2-in NAND equivalent).

Technology	Cell Area Gate eq.	Fmax
0.09µm	17 000	250MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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