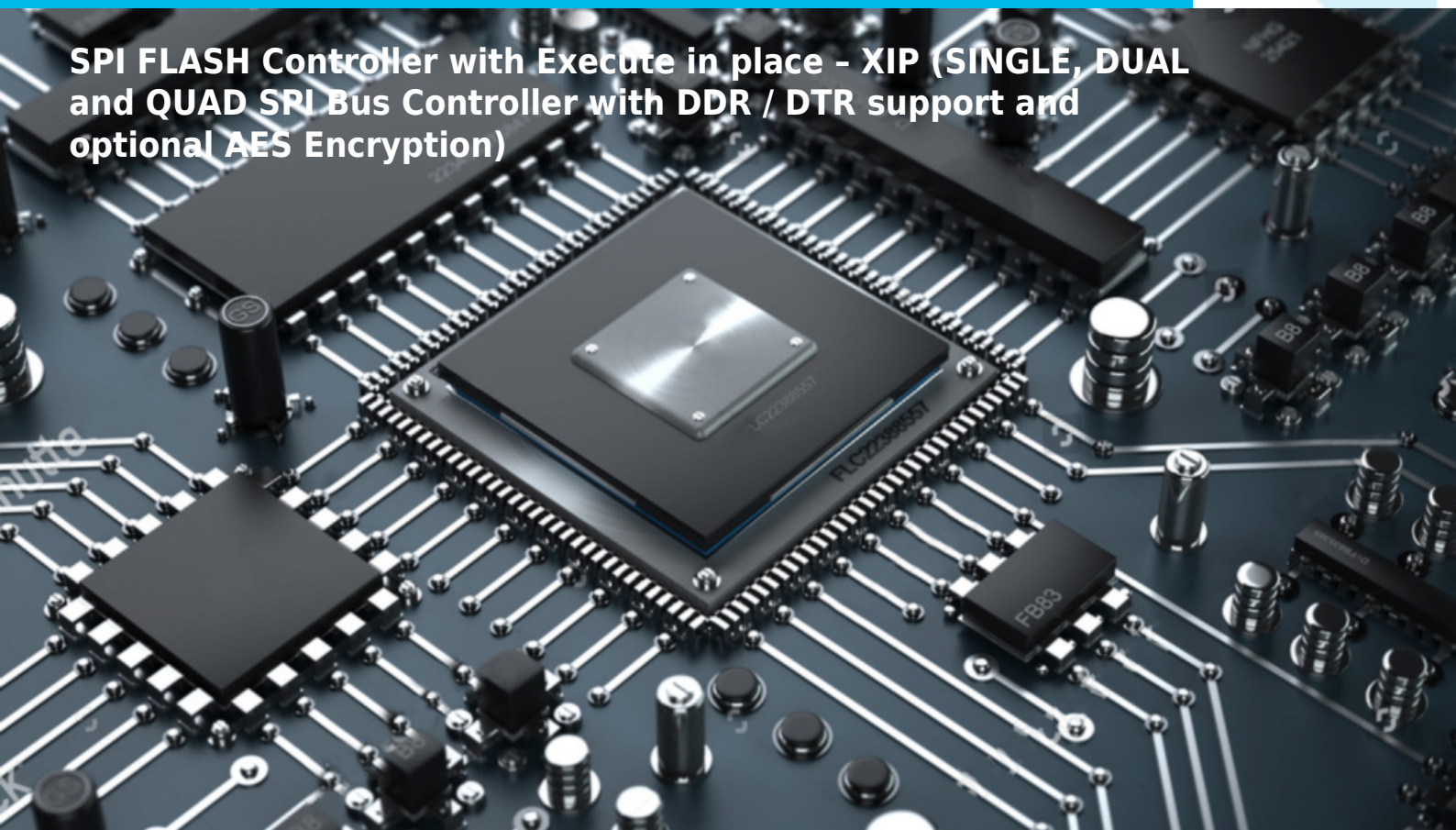
DIGITAL CORE DESIGN

HYPERBUS™ MEMORY CONTROLLER IP

SPI FLASH Controller with Execute in place – XIP (SINGLE, DUAL and QUAD SPI Bus Controller with DDR / DTR support and optional AES Encryption)



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

HyperBus™ Memory Controller IP Core — High-Performance SPI Master/Slave with HyperBus™ & xSPI Support

DCD-SEMI's **HyperBus™ Memory Controller IP Core** is a high-speed, fully configurable SPI master/slave solution, designed for seamless integration into modern **SoC** and **FPGA** architectures. Building on the proven DFSPI core, this IP bridges easily to **APB, AHB, and AXI buses**, supporting **SINGLE, DUAL, QUAD, and OCTAL SPI modes** for maximum design flexibility.

Optimized for **HyperBus™ memory** and **xSPI (JESD251A) standards**, the controller enables high-performance communication with **HyperRAM™** and NOR/NAND Flash memories. Designers benefit from fine-grained control over **serial clock polarity and phase (SCK)**, ensuring compatibility with a wide range of SPI peripherals.

Key Features & Benefits:

- **HyperBus™ and xSPI support** for next-generation memory interfaces
- **Flexible SPI modes**: SINGLE, DUAL, QUAD, OCTAL
- **Bridges APB, AHB, AXI buses** for easy SoC integration
- **Fully programmable SCK parameters** for custom clocking requirements
- **Automatic Slave Select control** via SSCR register
- **Technology-independent HDL design** deployable on ASIC and FPGA
- **DMA support** with single and multi-transfer modes for low-latency operation
- **Customizable configuration** tailored to system design needs

This **high-speed HyperBus™ memory controller** IP Core provides reliable, low-pin-count memory access for **embedded applications**, **high-performance SoCs**, and **FPGA-based designs**. With DCD-SEMI's emphasis on **robust, standards-compliant IP cores**, developers can achieve maximum **throughput, flexibility, and integration ease** for memory-intensive systems.

Ideal for designs requiring a **HyperBus memory controller IP package**, this IP core simplifies communication with popular SPI Flash memories while offering robust support for high-speed, low-pin-count HyperRAM™ devices. Backed by DCD-SEMI's reliability and customization flexibility, this IP core ensures optimal performance across a wide range of applications.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

DCD-SEMI SPI IP Cores

	DSPI	DQSPI	DOSPI	DFSPI	DOSPIS	DESPI	DESPIS
SPI mode	SINGLE	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD
Operation mode	Master only	Master only	Master only	Master only	Slave only	Master only	Slave only
Data rate	Low	Middle	High	High	High	Middle	Middle
Cost / complexity	Low	Middle	Middle	High	Middle	High	High
XIP support	Optional	Optional	Optional	Yes	No	No	No
DDR support	Yes	Yes	Yes	Yes	No	No	No
Standard supported	xSPI partially	xSPI partially	xSPI partially	xSPI, HyperBus, XCELLA	xSPI partially	Intel eSPI 1.6	Intel eSPI 1.6
Best option for	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller (Flash, DRAM, PSRAM, HyperRAM and other), program code execution	Serial bus to parallel bus bridge, RAM connection to SPI interface	PC mother-boards	PC mother-boards

KEY FEATURES

- NOR & NAND Flash Memory Support
- Set of software-accessible control registers to execute any Flash memory command
- Supports any device clock frequency, polarity, and phase,
- Programmable baud rate generator,
- Built-in FLASH Commands decoder supports most popular FLASH devices,
- Optional built-in AES Encoder/Decoder
- DMA support
- Optional support for various SPI Bus Standards: HyperBus™, xSPI

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- Compliant with AMBA2 Specification, support APB, AHB, AXI bus interfaces
- Single, Dual, Quad, and OCTAL SPI transfer/reception
- Execute in place – XIP functionality support
- Data Bus Size configuration to 8, 16, or 32 bits wide
- Optional FIFO size extension
- Maximum supported Flash address range – 32 bits
- Up to 4 SPI slaves can be addressed
  - Software Slave Select Output – SSO – selection
  - Automatic Slave Select outputs assertion
- System error detection
- Interrupt generation
- Bit rates generated as 1/ 2.. 1/255 of the system clock.
- Four SPI transfer formats supported: CPOL/CPHA.
- Simple interface allows easy connection to microcontrollers
- Fully synthesizable, static synchronous design with no internal tri-states

UNIT SUMMARY

Shift Register – The heart of the DFSPI controller. It shifts in and out data from the DFSPI controller regarding to the appropriate edge of the SCK.
Receiver FIFO – The Rx FIFO by default is 256 Bytes deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if interrupt is enabled, the DFSPI will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full and will not accept any next byte. Once the RX FIFOO is full, internal logic stops SPI operations to prevent FIFO overflow.
Transmitter FIFO – The DFSPI transmits data through DQ lines as soon as the CPU loads data into the Tx FIFO. When the TX FIFO is full, DFSPI prevents any further loads into it. When the next TX FIFO load occur, data is not written and the TX OVERFLOW error flag is set. Loading next data to the Tx FIFO will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.
Baudrate Generator – Used to generate the master SCK Clock in selected rate. System allows flexible SCK rate definition in range of CLK / 2 up to CLK/256, depending on the value written to the BauRate Register.
SPI Clock Logic – This module controls phase and polarity of generated/received SCK signal. On correct SCK edge generates shift signal to SPI Shift register.
System Bus Wrapper – Allows connection of the DFSPI CPU interface to peripheral Bus of the SoC system.
FLASH Commands decoder – The decoder recognizes the command code and set the transfer/reception parameters accordingly. Decoder supports most commands of the major FLASH types. For specific commands or memories user can switch the decoder off, then all the parameters need to be set manually. With decoder disabled, the DFSPI can support any FLASH and all the possible commands types.
AES Encoder / Decoder – This is an optional module, added as special request. The AES module allows the FLASH data to be encrypted with selected AES 128 or AES 256 encryption standards. With the AES module, all encryption operations are done fully automatic and do not require special effort during programming and XIP operations. The AES module is intended for applications with high code security demand. AES require the data buffer with the size of 64 bytes. With AES module all FLASH read/write operations require more time needed for the encryption process.

XIP – EXECUTE IN PLACE MODE

In the XIP mode, the DFSPI allows direct Read or Write of data from SPI FLASH memories. In this mode the DFSPI operates as a serial-to-parallel converter between SPI flash and CPU. To operate in the XIP mode, the SPI Flash needs to be configured first. Once it is correctly configured, XIP operation with DFSPI is ready just after power-up, without any further software effort. Default setting of the DFSPI Controller allows FLASH read using the preset READ Command just after power up. Other, specific commands or memory settings, require to be set in software first, or defined as default values before the DFSPI Controller synthesis. After memory configuration the memory space can be easily read through the DFSPI. For communication optimization, the DFSPI allows easy protocol configuration using XIP Control registers bits, allowing XIP operation without any software overhead.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Technology	Optimization	Gates	F_{max}
0.18 typical	area	4 900	160 MHz
0.18 typical	speed	6 000	400 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users

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to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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