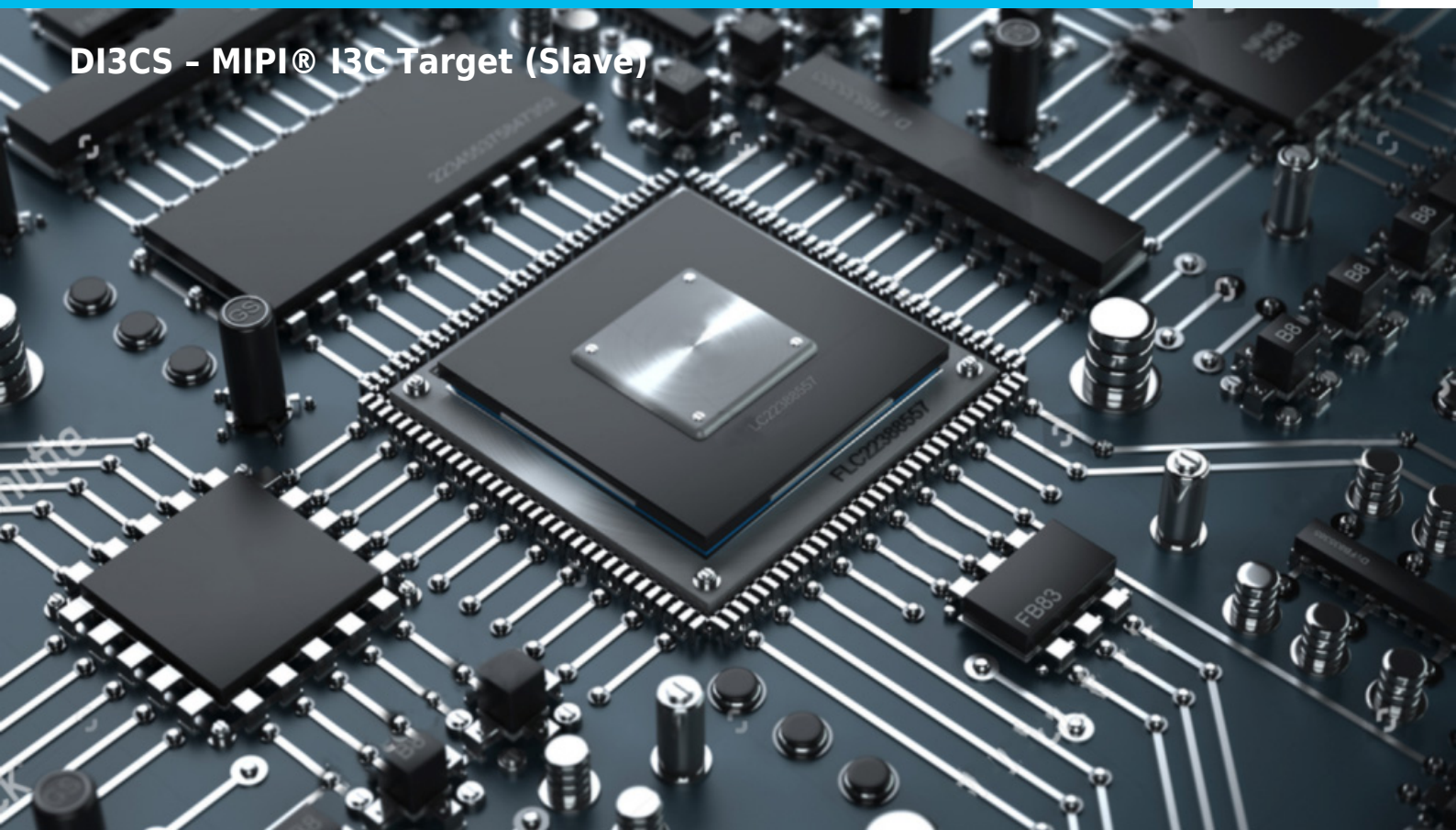
DIGITAL CORE DESIGN

DI3CS – MIPI® I3C TARGET (SLAVE)



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI3CS — Smart I3C Target (Slave)

Connectivity for Mobile, IoT, Automotive & Next-Gen Embedded Systems

The **DI3CS** is a high-performance **MIPI® I3C Target Controller IP Core** designed to bring efficient, high-speed, and low-power connectivity to modern embedded systems. Fully compliant with the **MIPI I3C Basic Specification**, it serves as a smart peripheral device communicating seamlessly with any I3C Master over the I3C bus.

Built as an evolution of the legacy I²C interface, the I3C protocol delivers **higher data rates, improved power efficiency, dynamic addressing, and better scalability**, making DI3CS an ideal choice for compact, sensor-rich applications in **mobile devices, IoT nodes, automotive subsystems, industrial electronics, and wearables**.

Feature-Rich, Specification-Compliant I3C Target IP

The DI3CS implements all mandatory functions defined by the **I3C Basic specification**, along with several advanced optional capabilities. Its architecture ensures easy integration into complex SoC, ASIC, and FPGA environments.

Key Supported Features

- **Single Data Rate (SDR)** and **Double Data Rate (DDR)** modes
- **Dynamic Address Assignment (DAA)** for flexible system configuration
- **In-Band Interrupts (IBI)** for efficient event signaling
- **Hot-Join** support for dynamic device insertion
- **Common Command Codes (CCC) execution**
- **Error detection**, recovery mechanisms, and **Target Reset** functionality
- **Backward compatibility with I²C**, enabling mixed-protocol environments

Optimized for High-Speed, Low-Power Embedded Designs

With its efficient implementation and flexible feature set, the DI3CS enables:

- **Fast, reliable communication** in data-intensive sensor networks
- **Low-power operation**, ideal for battery-driven IoT and wearable applications
- **Robust interoperability** with existing I3C ecosystems
- **Future-proof performance** aligned with next-generation embedded architectures

Whether you are designing **mobile sensors**, **environmental monitors**, **automotive peripherals**, or **industrial controllers**, the DI3CS IP Core ensures high bandwidth, reduced power consumption, and seamless integration.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

Why DI3CS?
With DI3CS, DCD-SEMI provides a forward-looking IP Core that enhances performance, reduces pin count and power usage, and simplifies integration across heterogeneous systems. Backed by decades of experience and top-tier technical support, DI3CS is your bridge to building **connected, intelligent, and future-ready devices**.

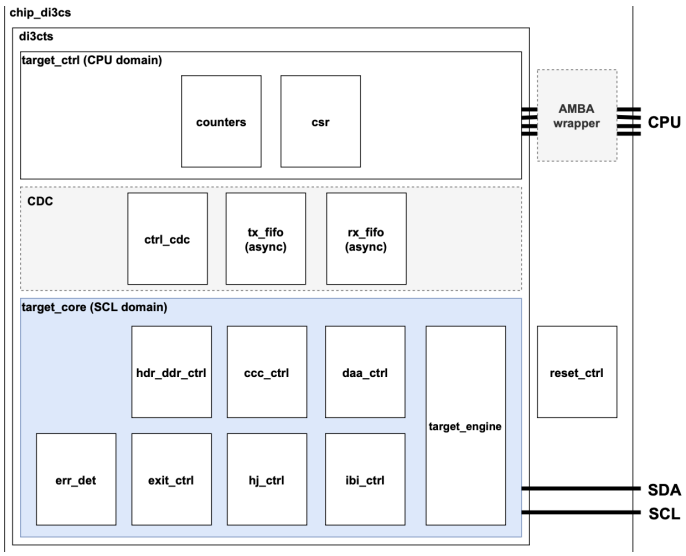
For further details, email info@dcd-semi.com

KEY FEATURES

- MIPI I3C Basic Specification v1.2 compiliance
- DI3CS – MIPI® I3C Target (Slave)
- Native 32-bit CPU Interface
- Optional CPU interface wrappers (APB, AHB, AXI)
- Legacy I2C communication with 7-bit Static Address
- I3C Single Data Rate (SDR) mode
- Double Data Rate (DDR) suport
- Dynamic Adress Assigment (DAA) supprot
- Common Command Codes (CCC) execution
- In-Band Interrupts (IBI) suport
- Hot-Join (HJ) support
- Target Reset mechanism supprot
- TE0-TE6 Errors detection and recovery (SDR)

- Frame, parity, CRC, data errors detection and recovery (DDR)
- Configurable Asynchronous RX FIFO
- Configurable Asynchronous TX FIFO
- Masked interrupts

BLOCK DIAGRAM



PERFORMANCE

For precise LATTICE performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

APPLICATIONS

The I3C was initially intended for mobile applications as a single interface that can be used for any sensor. Modern smartphones that include a multitude of sensors and a slew of supporting logic lines are pushing the boundaries of both I²C and SPI. That's why I3C accommodates many sensors on the same communication bus, while eliminating additional logic signals needed to support interrupt or sleep mode functionality. Of course, The DI3CS Core is useful for other applications than smartphones. It offers high speed data transfer at very low power levels, which is highly desirable for any embedded system. One of the examples are wearables (where multiple sensors are used in a very limited physical space and with stringent power restrictions). And if it's not enough it's worth to mention that DCD's IP Core as a standardized sensor interface can be utilized as a bus communication standard for touch sensing, always-on and low resolution cameras, acoustics, environmental sensors and transducers that currently use I²C, SPI, UART and others:

- Smartphones, tablets and laptops,
- IoT,
- Medical, health & fitness,
- Autonomous vehicles and ADAS,
- Embedded microprocessor boards,
- Low-power applications,
- Communication systems etc.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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