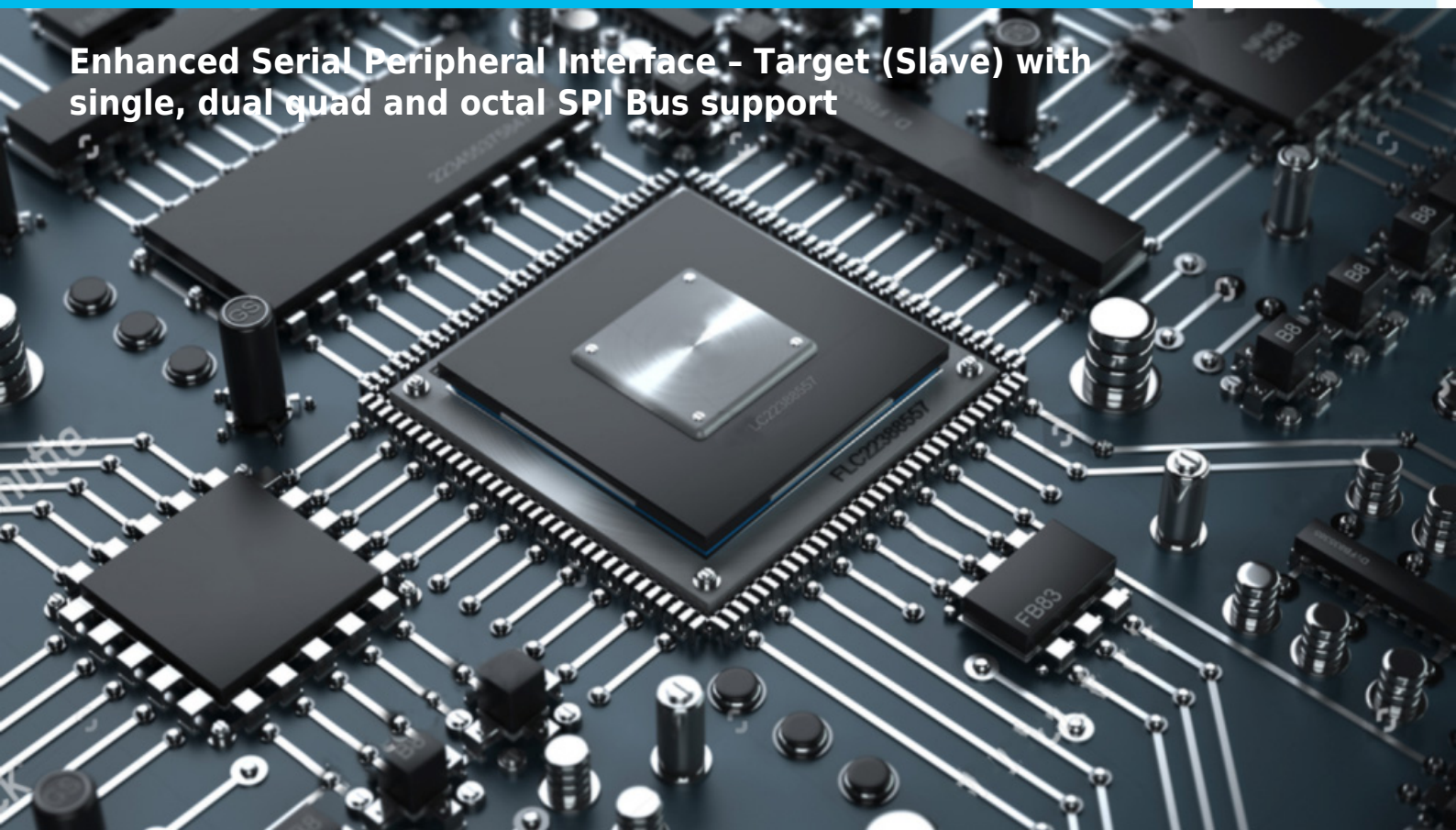
DIGITAL CORE DESIGN

DESPI TARGET IP

Enhanced Serial Peripheral Interface – Target (Slave) with single, dual quad and octal SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DESPI eSPI IP Core – Configurable High-Speed eSPI Target IP for FPGA and ASIC Designs

The DESPI IP Core is a fully configurable Enhanced Serial Peripheral Interface (eSPI) Target IP, compliant with the eSPI Base Specification Revision 1.6. It is designed for high-performance embedded systems, enabling reliable and efficient communication between microcontrollers, embedded controllers (EC), and eSPI-enabled peripherals in Intel-based platforms.

As a modern replacement for the legacy LPC bus, the DESPI IP Core delivers high-speed serial communication with support for single, dual, and quad SPI modes. It operates at serial clock frequencies up to 66 MHz, ensuring low-latency data transfer and optimized system throughput.

Its scalable and flexible architecture allows seamless integration into FPGA and ASIC designs, supporting both single and multi-Target configurations across a wide range of System-on-Chip (SoC) applications.

Key Features

- eSPI Target IP compliant with eSPI Base Specification Rev. 1.6
- Configurable Target mode (single or multiple Target devices) for complex system architectures (looking for an eSPI Controller? here it is)
- High-speed SPI interface up to 66 MHz for low-latency communication
- Support for Single, Dual, and Quad SPI transfers to maximize bandwidth
- Large, highly configurable shared memory buffer enables efficient and flexible frame and data storage to fit any needs.
- Customizable peripheral channels, including memory-mapped I/O, Virtual Wire signals, and event handling
- Technology-agnostic RTL design compatible with all major FPGA and ASIC vendors
- Optimized for integration into Intel-based systems and embedded controller environments

Typical Applications

- Embedded Controllers (EC) in Intel CPU platforms
- FPGA and ASIC-based SoC designs requiring eSPI connectivity
- High-speed data acquisition systems and industrial peripherals
- Multi-Target microcontroller systems with low-latency communication requirements
- Replacement of legacy LPC interfaces in modern hardware architectures

The DESPI eSPI IP Core is fully customizable to meet specific system and integration requirements, making it a reliable solution for next-generation embedded systems and high-performance digital designs.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

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DCD-SEMI SPI / eSPI IP Cores

	DSPI	DQSPI	DOSPI	DFSPI	DOSPIS	DESPI-C	DESPI-T
SPI mode	SINGLE	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD
Operation mode	Master only	Master only	Master only	Master only	Slave only	Master only	Slave only
Data rate	Low	Middle	High	High	High	Middle	Middle
Cost / complexity	Low	Middle	Middle	High	Middle	High	High
XIP support	Optional	Optional	Optional	Yes	No	No	No
DDR support	Yes	Yes	Yes	Yes	No	No	No
Standard supported	xSPI partially	xSPI partially	xSPI partially	xSPI, HyperBus, XCELLA	xSPI partially	Intel eSPI 1.6	Intel eSPI 1.6
Best option for	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller (Flash, DRAM, PSRAM, HyperRAM and other), program code execution	Serial bus to parallel bus bridge, RAM connection to SPI interface	PC motherboards	PC motherboards

KEY FEATURES

- Compliant with eSPI base specification as defined in Enhanced Serial Peripheral Interface (eSPI) Specification rev.1.6
  - Supports Slave Mode
  - Supports Single, Dual and Quad modes
  - Supports TX and RX operation as per specs
  - Support for
    - Command Phase
    - Turn-Around Phase
    - Response Phase
  - Baud Rate selection
  - Slave Triggered Transactions
  - Power management Event
  - Interrupts and Alerts
  - In-band reset
  - Support for multiple channels
    - Peripheral channel
    - Virtual wire Channel
    - OOB Message (Tunneled SMBus) Channel
    - Run-time Flash Access Channel
  - Various Master/Slave errors detection
  - CRC Checking and generation
  - Simple interface allows easy connection to microcontrollers
  - Fully synthesizable, static synchronous design with no internal tri-states

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

BLOCK DIAGRAM

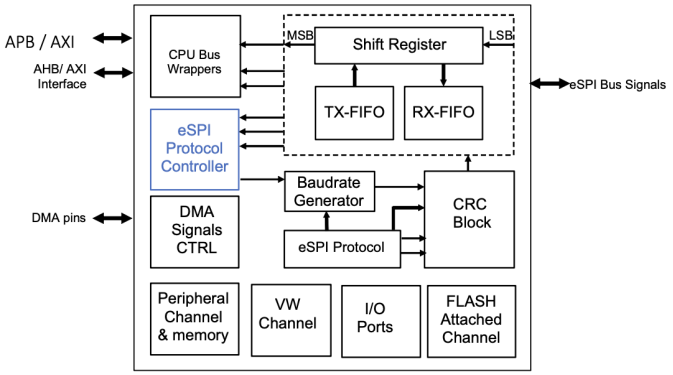

Figure 4. DESPI Block Diagram

PERFORMANCE

For precise MICROSEMI performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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