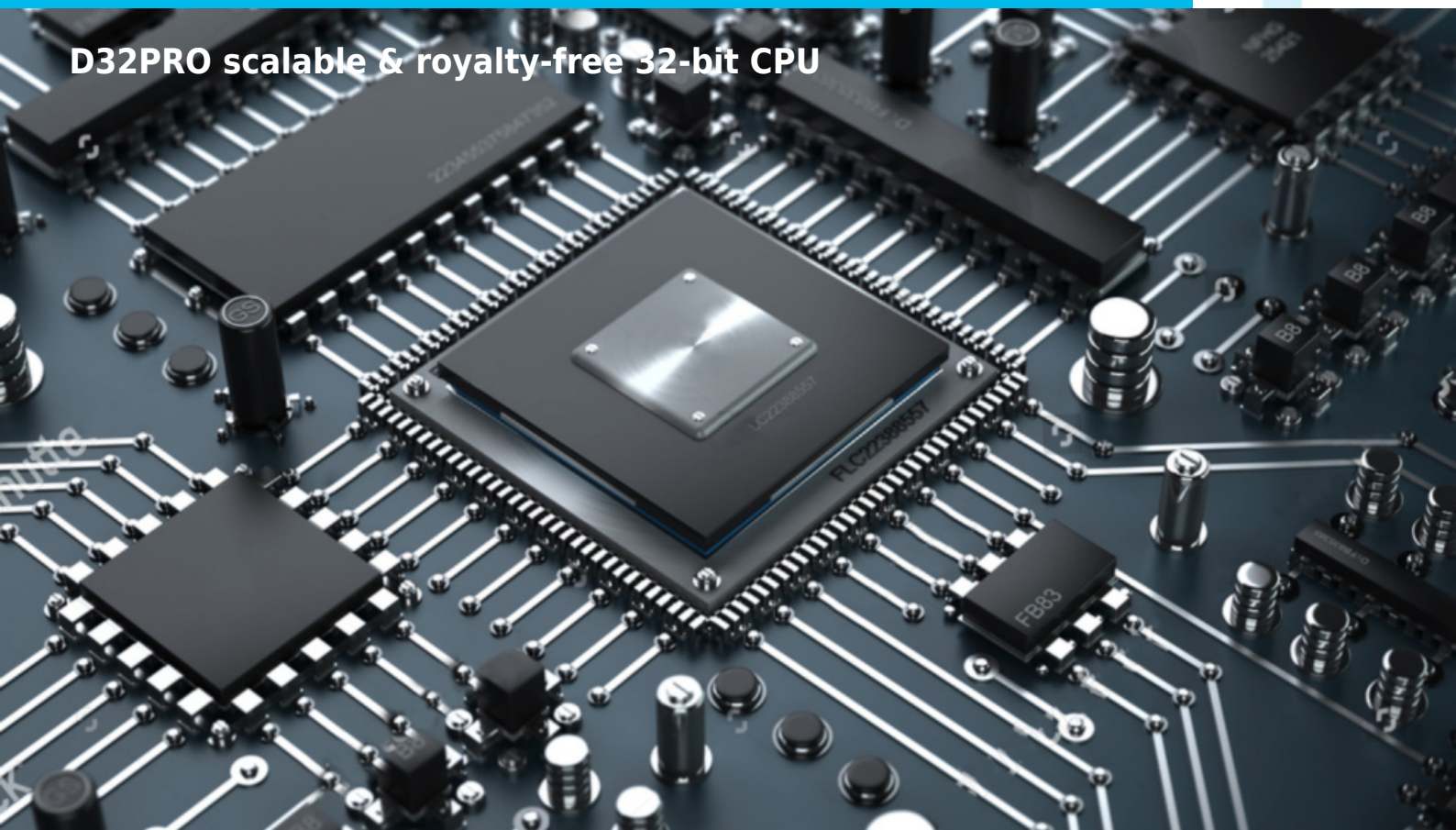
DIGITAL CORE DESIGN

D32PRO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

Thanks to its **increased code density**, the D32PRO meets the power and size requirements of new connected devices. That's why both the power and performance of this IP Core predestine it as a **real alternative for ARM Cortex M0/M0+/M1/M3** in the **deeply embedded** market and especially for the emerging market of connected devices (IoT). Responding to continuing demands for less power drain in system-on-chip (SoC) designs, DCD has developed the instruction set aimed at reducing the size of the system's instruction memory. The D32PRO is aimed at low-power always on/always listening systems and those with less demanding clock frequencies such as Bluetooth Low Energy. Nevertheless, the core is **perfect for embedded systems that require greater computational performance** and system complexity by supporting dual- and multi-core systems as well as improved code density. DCD's IP Core is fully customizable – it is delivered in an exact configuration to meet your requirements. The D32PRO comes with a **wide variety of peripherals,** like USB, SPI, LCD, HDLC, UART, Ethernet MAC, CAN, LIN, RTC, and many more – ready to be implemented with the CPU. The D32PRO is delivered with a fully automated test bench and a complete set of tests, allowing easy package validation at each stage of SoC design.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

CPU FEATURES

- Configurable 32-bit Harvard architecture
- Performance up to **1.52 / 2.67 DMIPS/MHz** and **2.59 CoreMarks/MHz**
- Small footprint starting at **10.6k/6.8k** ASIC gates
- Very high clock frequency up to 1 GHz in modern ASIC technologies
- Fifteen 32-bit general Purpose registers
- ASIC Silicon proven architecture
- Up to 256 MB of Code Space with encrypted bootloader
- Up to 256 MB of Data Space
- Built-in configurable Floating Point co-processor using dedicated instructions
- Configurable 32-bit hardware multiplier
- Configurable 32-bit hardware divider
- Configurable 32-bit hardware shifter
- Low power consumption by Advanced Power Management Unit
  - Advanced Power management mode
  - Switchback feature
  - Stop mode
- Configurable Interrupt Controller
  - Non Maskable Interrupt
  - Up to 16 priority levels
  - Up to 32 external interrupt sources
- System clock controller supporting
  - Phase Locked Loops (PLL)
  - external clock generator
  - on-chip clock oscillator
- DoCD™ on-chip debug unit
  - Processor execution control
    - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - System Space
    - Program Memory Space
    - Data Memory Space
    - Peripherals Space
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoints at
    - Data Memory Space
    - Program Memory Space
    - Peripherals Space
    - System Space
  - Hardware watchpoints activated at a certain
    - address by any write into any Space
    - address by any read from Space
    - address by write into space a required data
    - address by read from space a required data
  - Hardware watchpoint windows activated at a certain
    - Start/stop address by any write into any Space
    - Start/stop address by any read from Space
    - Start/stop address by write into space a required data
    - Start/stop address by read from space a required data
  - 2-wire high-speed communication interface
- Ultimate dense code
- Great variety of peripherals
- AHB-Lite interface ready
- Rapid & easy development with ready to use tools
- Customization friendly with GUI

- Patent pending architecture
- Royalty-free

SOFTWARE DEVELOPMENT PLATFORM

- Eclipse Integrated Development Environment
- *GCC set of tools including C & C++ languages*
- *Debugger, Linker and Assembler*
- *Dedicated Simulator*
- *Supports Windows*
- Low cost USB debug cable
  - USB2 .0 High Speed cable (480 Mbps)
  - 2-wire high-speed DoCD interface

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CONFIGURATION

Several parameters of the D32PRO can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file or using GUI. There is no need to change any parts of the HDL code.

PERFORMANCE

To provide you with the most accurate and detailed insights about the ASIC performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVERABLES

The list of deliverables consists of:

- ASIC proven architecture
- Source code:
  - VERILOG Source Code or
  - FPGA Netlist
- VERILOG test bench environment
  - ModelSim automatic simulation macros
  - NCSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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