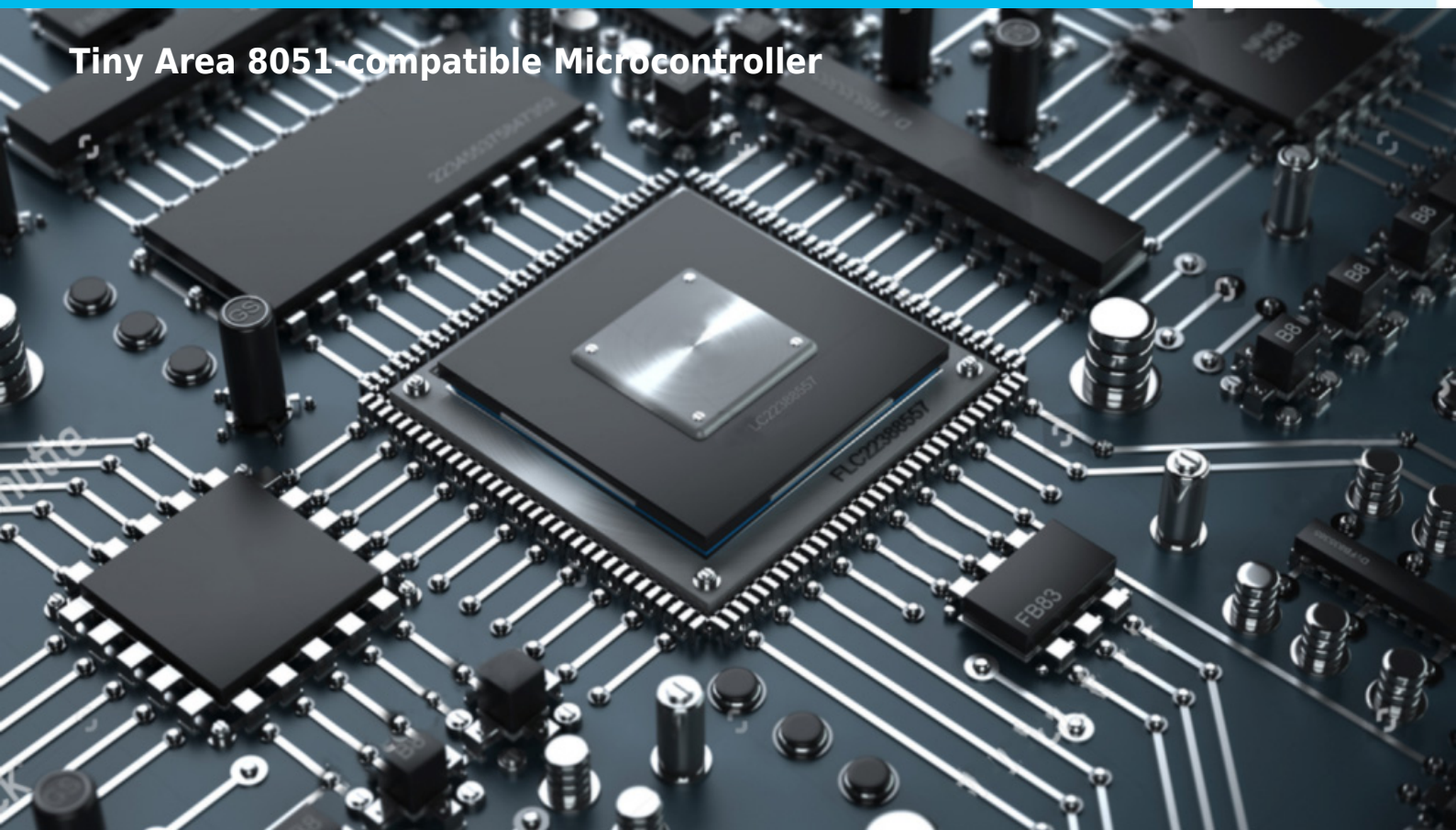
DIGITAL CORE DESIGN

DT8051

Tiny Area 8051-compatible Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DT8051 – **area optimized**, the tiny soft core of a single-chip 8-bit embedded microcontroller, based on the World's fastest and most popular DP8051 core available for over 18 years. The DT8051 softcore is 100% binary-compatible with the industry standard 8051 8-bit microcontrollers. It has a very low gate count architecture, giving 6 650 ASIC gates for the complete system, including the DoCD on-chip debugger. Dhrystone 2.1 benchmark program runs exactly **8.1 times faster** than the original 80C51 at the same frequency. The same C compiler was used for benchmarking the core vs 80C51, with the same settings. The DT8051 includes a 2-wire DoCD on-chip debugger (TTAG™), up to eight external interrupt sources, an advanced Power Management Unit, Timers 0&1, I/O bit addressable Ports, full duplex UART, and an interface for external SFR. The DT8051 Core has built-in support for the 2-wire TTAG™ interface – DCD's Hardware Debug System, called **DoCD™**. This version of the debugger is dedicated to applications where the number of external pins is limited. The DT8051 is delivered with **a fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each of DCD's 8051 Cores has built-in support for the Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger** that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, set breakpoints, and watchpoints, and read/write any contents of the microcontroller, including all registers, internal and external program memories, and all SFRs, including user-defined peripherals. More details about our on-Chip Debugger

Watch the DT8051 presentation on DCD's You Tube:

As Seen On YouTube

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

APPLICATIONS

- Low power battery operated devices
- Mixed signal systems
- Area optimized FPGA/ASIC design
- FSM replacements

CPU FEATURES

- Software compatible with the 8051 industry standard
- Very low gate count, area optimized architecture – 6 650 ASIC gates for a **complete system** with DoCD on-chip debugger
- 1 times faster than a standard 8051
- 63 VAX MIPS at 100 MHz
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64k bytes of internal (on-chip) Program Memory
- Up to 64k bytes of external (off-chip) Program Memory
- Up to 64k bytes of external (off-chip) Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Power Management Unit
  - Power management mode
  - Switchback feature
  - Stop mode
- Interrupt Controller
  - 2 priority levels
  - 8 external interrupt sources
  - 3 interrupt sources from peripherals
- 8-bit I/O Port
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- Two 16-bit timer/counters
  - Timers clocked by internal source
  - Auto reload 8-bit timers
  - Externally gated event counters
- Full-duplex serial port
  - 8-bit asynchronous mode, variable baud rate
  - 9-bit asynchronous mode, variable baud rate
- Interface for additional Special Function Registers
- **2-wire** DoCD™ debug unit
  - Processor execution control
  - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - two real-time PC breakpoints

    - unlimited number of real-time OPCODE breakpoints
  - Three independent Memory watchpoints
    - SFR, DATA, XDATA
    - **2-wire** TTAG communication interface
- Fully synthesizable, static synchronous design, with positive edge clocking and no internal tri-states
- Scan test ready

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BENEFITS

- Lowest gate count, 8051 compatible architecture
- Very low power consumption
- Significant performance improvement with respect to the 80C51 device, working at the same clock frequency (**1 in terms of Dhrystone MIPS**)
- On demand customization

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Control Unit – Performs core synchronization and data flow control. Connected directly to the Opcode Decoder, manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. Performs instructions code fetching. The whole program memory (FLASH or SRAM type) can be written by the DoCD™ debugger or the application can modify some part of its code – for example, storing some data which shouldn't volatile.
External Memory Interface – Contains memory access related registers, like Data Page High (DPH) and Data Page Low (DPL) registers. Performs memory addressing and data transfers.
Internal Data Memory Interface – Controls the access into the internal memory of size up to 256 bytes. Contains 8-bit Stack Pointer (SP) register and related logic.
SFR's Interface – Special Function Register interface manages communication between the CPU and user specified special registers.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Interrupt Controller – A module responsible for the interrupt manage system for the eight external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.
Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.
UART – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning, it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered so it can commence reception of second byte before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0, reads a physically separate receive register. It works in 2 asynchronous modes with variable baud rate, covering all standard transmission speeds.
Ports – Contains 8051's general purpose I/O ports. Each of port's pins can be read/written as a single bit or as an 8-bit bus.
DoCD™ Debug Unit – **2-wire, low gate count, real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the DoCD™ provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints control execution of program memory code; hardware watchpoints can be set and control internal and external data memories and SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins (CODERUN and DEBUGACS) indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by the DoCD™ debugger. The DoCD™ system includes **TTAG interface** and complete set of tools, to communicate and work with the core in real time debugging. It is built as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

PERFORMANCE

The following tables give a survey about the DT8051 and DoCD on-chip debugger area and performance in INTEL FPGA® Programmable Logic Devices (all features included).

Results given for a working system with SFR IDATA, CODE and XDATA memories.

Device	Speed grade	Area LE/ALM	F_{max}
CYCLONE-II	-6	1 666	95 MHz
CYCLONE-III	-6	1 656	100 MHz
STRATIX-II	-3	1 287 ALUT	155 MHz
STRATIX-III	-2	1 289 ALUT	210 MHz

DT8051 without the DoCD debugger

Device	Speed grade	Area LE/ALM	F_{max}
CYCLONE-II	-6	1 913	90 MHz
CYCLONE-III	-6	1 911	95 MHz
STRATIX-II	-3	1 507 ALUT	150 MHz
STRATIX-III	-2	1 508 ALUT	200 MHz

DT8051 with a compact version[1] of the DoCD debugger

Device	Speed grade	Area LE/ALM	F_{max}
CYCLONE-II	-6	2 088	80 MHz
CYCLONE-III	-6	2 093	95 MHz
STRATIX-II	-3	1 623 ALUT	135 MHz
STRATIX-III	-2	1 629 ALUT	185 MHz

DT8051 with full version[2] of DoCD debugger
1- compact DoCD version includes processor execution control (run, halt, reset, step); read-write all processor content (PC, SFRs); read-write all processor memories (IDATA, XDATA, CODE memory); FLASH code memory programming; one hardware code execution breakpoint; unlimited number of OPCODE execution breakpoints
2- full DoCD version includes processor execution control (run, halt, reset, step); read-write all processor content (PC, SFRs); read-write all processor memories (IDATA, XDATA, CODE memory); FLASH CODE memory programming; two hardware code execution breakpoints; six configurable hardware watch-points (IDATA, XDATA, SFRs); unlimited number of OPCODE execution breakpoints

Dhrystone Benchmark Version 2.1 was used to measure the Core performance. The following table gives a survey about the DT8051 performance in Dhrystone/sec and VAX MIPS rating per 1 MHz (DMIPS/MHz).

Device	Dhry/sec [12 MHz]	DMIPS/MHz	80C51 ratio
80C51	197	0,0094	1,00
DT8051	**1 597**	**0,0763**	**8,11**

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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