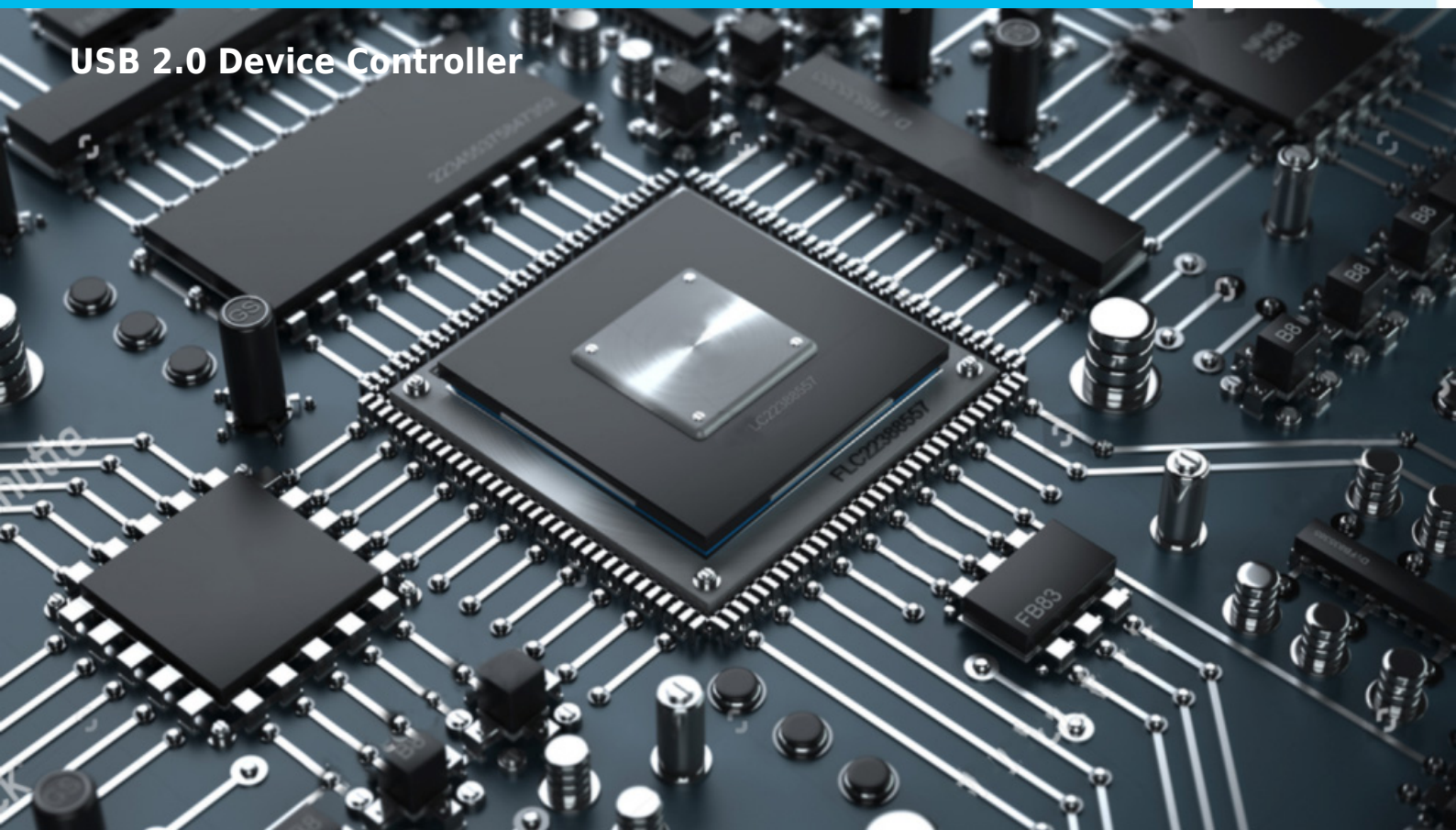
DIGITAL CORE DESIGN

DUSB2

USB 2.0 Device Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DUSB2 – Full/High-Speed USB 2.0 Peripheral Controller IP Core

The **DUSB2** is a **hardware implementation of a USB 2.0 full/high-speed peripheral controller** that interfaces with a UTMI bus transceiver. This IP core provides a robust and efficient solution for FPGA and ASIC designs, handling all **USB packet processing, PID and address recognition, endpoint management, and FIFO control logic**.

Key Features:

- Supports **12 Mb/s Full-Speed (FS)** and **480 Mb/s High-Speed (HS)** USB 2.0 operation.
- Interfaces seamlessly with **UTMI bus transceivers**.
- Includes PID and address recognition logic for accurate USB communication.
- State machines manage USB packets and transactions efficiently.
- Endpoint number recognition logic and FIFO control for optimized data buffering.
- **Technology-independent design** suitable for multiple process technologies.
- Fully compliant with **USB Specification v2.0**.
- Delivered with a **complete automated test bench** for rapid SoC integration and validation.

Benefits for Engineers:

- Simplifies USB 2.0 peripheral integration in **FPGA or ASIC designs**.
- Reduces CPU overhead by offloading USB packet and endpoint processing to hardware.
- Accelerates development with fully validated RTL and automated test suites.
- Ensures compliance with USB standards for reliable device operation.

Ideal Applications:

- USB 2.0 peripherals for embedded systems
- Mass storage and communication devices
- Custom USB interface designs in FPGA or ASIC

DUSB2 provides engineers with a **ready-to-use, high-performance USB 2.0 peripheral controller** that minimizes design complexity and accelerates time-to-market.

USB IP Core	USB Version	Bus Interface	CPU / MCU	Software Stack	Debug Tools	Key Features	Ideal Applications
MS Platform	USB 2.0 Full/High-Speed	APB, AHB, AXI	DP8051XP 8-bit MCU	HID software stack optimized for DP8051XP	HAD2 Debugger, DoCD™ software, Keil & IAR drivers	Complete HID design solution, preprogrammed FPGA example, ready-to-use	Mice, keyboards, tablets, other HID devices
DUSB2	USB 2.0 Full/High-Speed	APB, AHB, AXI	Standalone or host MCU	N/A	DoCD™ optional	Full/high-speed controller, ULPI support, ready-to-use RTL	General USB 2.0 devices, mass storage, communication peripherals
DUSB2-ULPI	USB 2.0 High-Speed	APB, AHB, AXI	Standalone or host MCU	N/A	DoCD™ optional	ULPI-compliant high-speed controller, optimized for external PHY integration	Devices requiring ULPI PHY, high-speed USB
USB 2.0 HID Design Platform	USB 2.0 Full/High-Speed	APB, AHB, AXI	DP8051XP 8-bit MCU	HID software stack	HAD2 Debugger, DoCD™ software, Keil & IAR drivers	Turnkey HID solution, preprogrammed example, easy FPGA integration	Mice, keyboards, tablets, game controllers
USB 2.0 Audio Design Platform	USB 2.0 Full/High-Speed	APB, AHB, AXI	DP8051XP 8-bit MCU	Audio software stack	HAD2 Debugger, DoCD™ software, Keil & IAR drivers	Ready-to-use audio solution, preprogrammed FPGA example	USB microphones, speakers, audio interfaces

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation

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- Software configurable EP0 control endpoint size 8-64 bytes
- Software configurable 15 IN/OUT end-points:
  - configurable number of endpoints
  - configurable type of each endpoint: INTERRUPT, BULK or ISOCHRONOUS
  - configurable direction of each endpoint
  - configurable size of each endpoint: 8-1024 bytes
- Supports UTMI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- Simple interface allows easy connection to CPU
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

CONFIGURATION

At the synthesis level, the following parameters of the DUSB2 core can be easily adjusted to requirements of a dedicated application and technology. The CPU interface is configurable as 8, 16 or 32-bit wide. Each data endpoint can be effortlessly enabled and disabled, by simply changing an appropriate constant in the package file. There is no need to change any parts of the code, to prepare DUSB2 core with requested number of data endpoints.

- EP1_ENABLE – *TRUE (1)/FALSE (0)*
- EP2_ENABLE – *TRUE (1)/FALSE (0)*
- EP3_ENABLE – *TRUE (1)/FALSE (0)*
- EP4_ENABLE – *TRUE (1)/FALSE (0)*
- EP5_ENABLE – *TRUE (1)/FALSE (0)*
- EP6_ENABLE – *TRUE (1)/FALSE (0)*
- EP7_ENABLE – *TRUE (1)/FALSE (0)*
- EP8_ENABLE – *TRUE (1)/FALSE (0)*
- EP9_ENABLE – *TRUE (1)/FALSE (0)*
- EP10_ENABLE – *TRUE (1)/FALSE (0)*
- EP11_ENABLE – *TRUE (1)/FALSE (0)*
- EP12_ENABLE – *TRUE (1)/FALSE (0)*
- EP13_ENABLE – *TRUE (1)/FALSE (0)*
- EP14_ENABLE – *TRUE (1)/FALSE (0)*
- EP15_ENABLE – *TRUE (1)/FALSE (0)*

Besides synthesis level configuration parameters mentioned above, there is a portion of device and endpoints parameters configured at software level, after the USB bus reset condition. The following parameters can be configured at software level:

- Endpoint 0 FIFO size to 8, 16, 32 or 64 bytes
- Endpoints 1-15 FIFO size to 8, 16, 32, 64, 128, 256, 512 or 1024 bytes
- Endpoints 1-15 direction to IN or OUT
- Endpoints 1-15 mode to INTERRUPT, BULK or ISOCHRONOUS

UNITS SUMMARY

UTMI Interface – Clocked by UTMICLK clock and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.
CPU Interface – Clocked by CPUCLK clock and manages communication with some CPU. In this module DUSB2 core configuration and status registers are being located. CPU bus size is configurable as 8, 16 or 32-bit wide.
SRAM Interface – Manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.
EP0 endpoint – A special bidirectional endpoint, used for device configuration. It allows generic USB control and status access.
EP1-EP15 endpoints – Unidirectional configurable double-buffered endpoints, used for application specific data transmission.

APPLICATIONS

- Human Interface Devices like keyboards, mousses or game peripherals
- Mass Storage devices like flash disks, mp3 or mp4 players
- GPS navigation systems
- Digital Cameras
- Cellular phones
- Audio devices like microphones and speakers
- Printers
- Scanners

PERFORMANCE

The following tables give a survey about the Core area and performance in **INTEL** Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed grade	cpuclk F_{max}	utmiclk F_{max}
CYCLONE-II	-6	150 MHz	>100 MHz
CYCLONE-III	-6	180 MHz	>100 MHz
STRATIX-II	-3	250 MHz	>100 MHz
STRATIX-III	-2	270 MHz	>100 MHz
Arria GX	-6	200 MHz	>100 MHz

Core performance in INTEL FPGA® devices

The area utilized by typical configuration of the DUSB2 core suitable for HID and Mass Storage devices in vendor specific technologies, is summarized in the following table.

Component	Area	
	[LE]	[FFs]
CPU interface	270	170
UTMI interface	310	230
SRAM interface	130	95
EP0 endpoint	180	140
EP1 endpoint	190	155

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EP2 endpoint	190	155
Total area	**1 270**	**945**

Core components area utilization in STRATIX-II, STRATIX-III and Arria GX families.

Component	**Area**	
	[LE]	**[FFs]**
CPU interface	390	170
UTMI interface	450	230
SRAM interface	190	95
EP0 endpoint	260	140
EP1 endpoint	300	155
EP2 endpoint	300	155
Total area	**1 890**	**945**

Core components area utilization in CYCLONE-II and CYCLONE-III families

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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