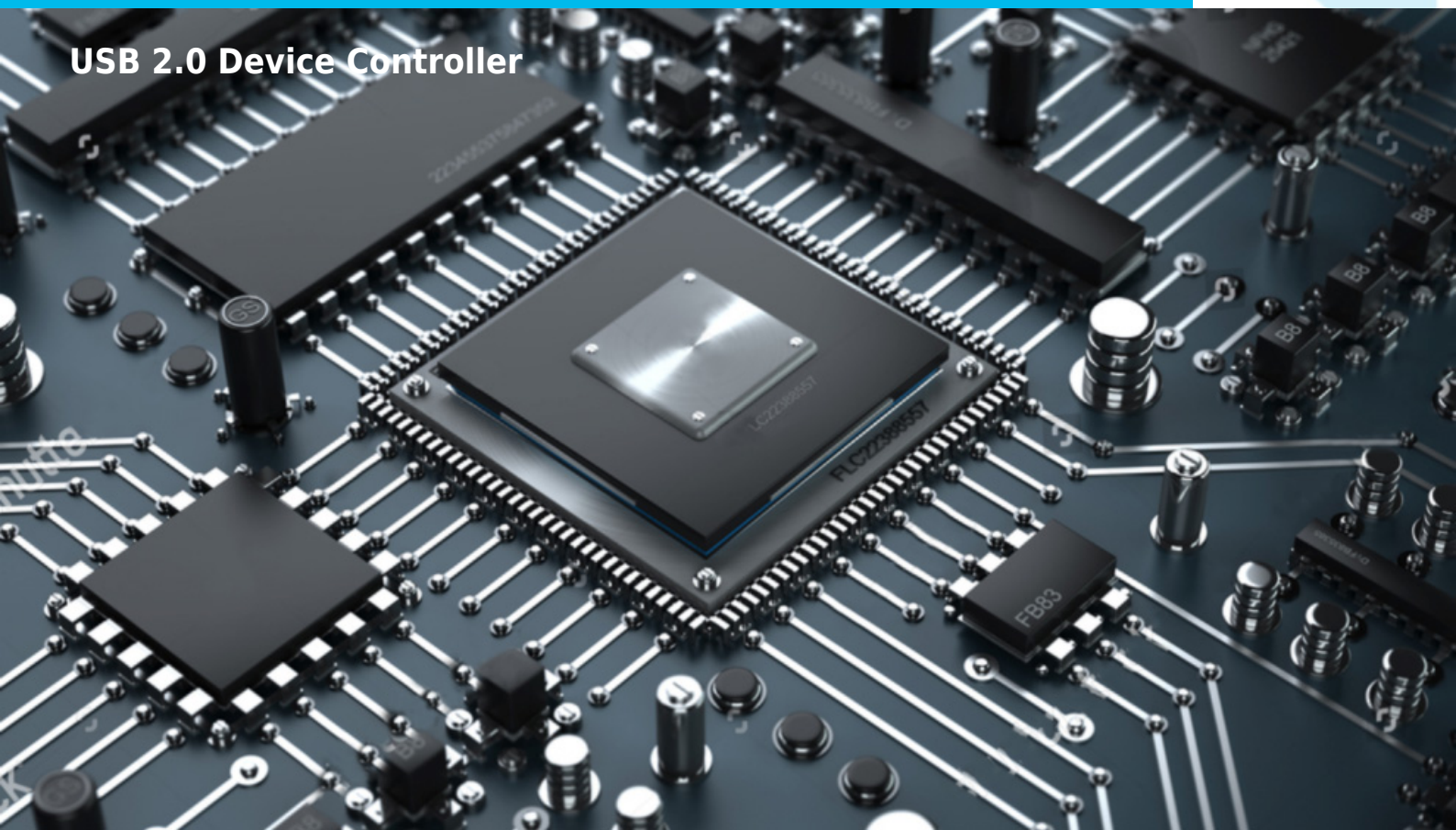
DIGITAL CORE DESIGN

DUSB2

USB 2.0 Device Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DUSB2 is a hardware implementation of a full/high-speed peripheral controller that interfaces to the UTMI bus transceiver. The IP Core contains the USB PID and address recognition logic, state machines to handle USB packets and transactions, endpoints number recognition logic and endpoints FIFO control logic.

The DUSB2 is **designed to support:**

- 12 Mb/s **"Full Speed"** (FS)
- 480 Mb/s **"High Speed"**(HS).

The **design is technology independent** and thus can be implemented in variety of process technologies. This core **strictly conforms to the USB Specification v2.0**. The DUSB2 core is **delivered with fully automated test bench and complete set of tests**, allowing easy package validation at each stage of SoC design flow.

KEY FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Software configurable EP0 control endpoint size 8-64 bytes
- Software configurable 15 IN/OUT end-points:
  - configurable number of endpoints
  - configurable type of each endpoint: INTERRUPT, BULK or ISOCHRONOUS
  - configurable direction of each endpoint
  - configurable size of each endpoint: 8-1024 bytes
- Supports UTMI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- Simple interface allows easy connection to CPU
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

CONFIGURATION

At the synthesis level, the following parameters of the DUSB2 core can be easily adjusted to requirements of a dedicated application and technology. The CPU interface is configurable as 8, 16 or 32-bit wide. Each data endpoint can be effortlessly enabled and disabled, by simply changing an appropriate constant in the package file. There is no need to change any parts of the code, to prepare DUSB2 core with requested number of data endpoints.

- EP1_ENABLE – *TRUE (1)/FALSE (0)*
- EP2_ENABLE – *TRUE (1)/FALSE (0)*
- EP3_ENABLE – *TRUE (1)/FALSE (0)*
- EP4_ENABLE – *TRUE (1)/FALSE (0)*
- EP5_ENABLE – *TRUE (1)/FALSE (0)*
- EP6_ENABLE – *TRUE (1)/FALSE (0)*
- EP7_ENABLE – *TRUE (1)/FALSE (0)*
- EP8_ENABLE – *TRUE (1)/FALSE (0)*
- EP9_ENABLE – *TRUE (1)/FALSE (0)*
- EP10_ENABLE – *TRUE (1)/FALSE (0)*
- EP11_ENABLE – *TRUE (1)/FALSE (0)*
- EP12_ENABLE – *TRUE (1)/FALSE (0)*
- EP13_ENABLE – *TRUE (1)/FALSE (0)*
- EP14_ENABLE – *TRUE (1)/FALSE (0)*
- EP15_ENABLE – *TRUE (1)/FALSE (0)*

Besides synthesis level configuration parameters mentioned above, there is a portion of device and endpoints parameters configured at software level, after the USB bus reset condition. The following parameters can be configured at software level:

- Endpoint 0 FIFO size to 8, 16, 32 or 64 bytes
- Endpoints 1-15 FIFO size to 8, 16, 32, 64, 128, 256, 512 or 1024 bytes
- Endpoints 1-15 direction to IN or OUT
- Endpoints 1-15 mode to INTERRUPT, BULK or ISOCHRONOUS

UNITS SUMMARY

UTMI Interface – Clocked by UTMICLK clock and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.
CPU Interface – Clocked by CPUCLK clock and manages communication with some CPU. In this module DUSB2 core configuration and status registers are being located. CPU bus size is configurable as 8, 16 or 32-bit wide.
SRAM Interface – Manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.
EP0 endpoint – A special bidirectional endpoint, used for device configuration. It allows generic USB control and status access.
EP1-EP15 endpoints – Unidirectional configurable double-buffered endpoints, used for application specific data transmission.

APPLICATIONS

- Human Interface Devices like keyboards, mousses or game peripherals
- Mass Storage devices like flash disks, mp3 or mp4 players
- GPS navigation systems
- Digital Cameras
- Cellular phones
- Audio devices like microphones and speakers
- Printers
- Scanners

PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route.

Family	Device	Speed grade	LUT	Slice	cpu F_{max}
Spartan-3	xc3s200	-5	1 671	1 310	121 MHz
Spartan-3E	xc3s250e	-5	1 694	1 327	135 MHz
Spartan-6	xc6slx4	-3	1 420	548	212 MHz
Virtex-4	xc4vfx12	-12	1 701	1 328	256 MHz
Virtex-5	xc5vlx20t	-2	1 423	810	300 MHz
Virtex-6	xc6vlx75t	-3	1 412	682	312 MHz
Virtex-7	xc7vx330t	-3	1 483	722	384 MHz
Kintex-7	xc7k70t	-3	1 492	704	384 MHz
Artix-7	xc7a100t	-3	1 388	695	263 MHz
Virtex UltraScale	xcvu065	-3	1 233	262	500 MHz
Zynq-7000	xc7z010	-3	1 232	482	330 MHz

Core performance in XILINX® devices

The area utilized by typical configuration of the DUSB2 core suitable for HID and Mass Storage devices in vendor specific technologies, is summarized in the following table.

Component	Area	
	[Slices]	[FFs]
CPU interface	225	170
UTMI interface	265	230
SRAM interface	115	95
EP0 endpoint	150	140
EP1 endpoint	160	155
EP2 endpoint	160	155
Total area	**1 075**	**945**

Core components area utilization in XILINX devices except VIRTEX-5 family

Component	Area	
	[Slices]	[FFs]
CPU interface	120	170
UTMI interface	145	230
SRAM interface	65	95
EP0 endpoint	80	140
EP1 endpoint	85	155
EP2 endpoint	85	155
Total area	**580**	**945**

Core components area utilization in XILINX VIRTEX-5 devices

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: 0048 32 282 82 66

fax: 0048 32 282 74 37
Please check: dcd.pl/contact-us/

Distributors: