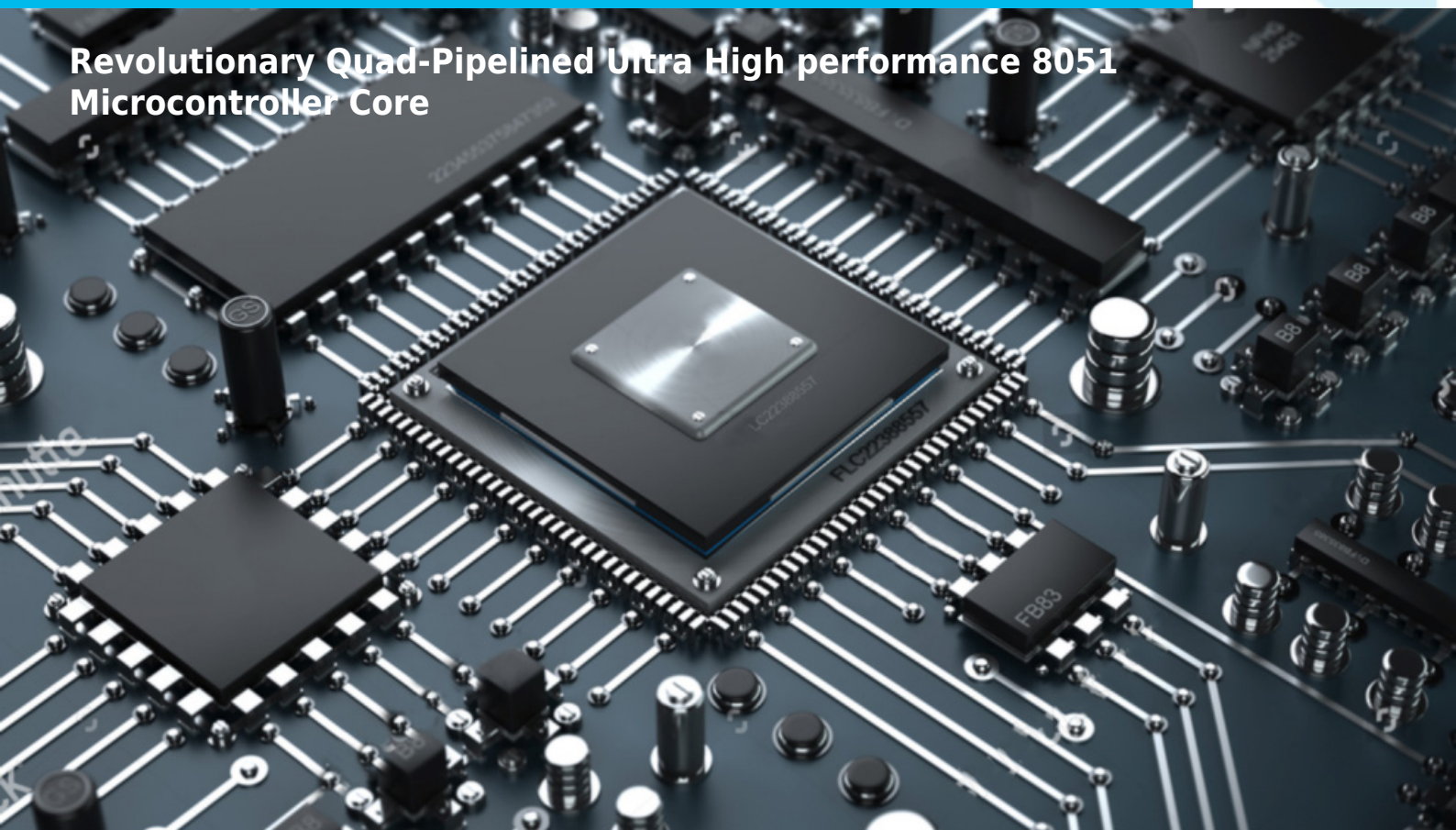
DIGITAL CORE DESIGN

DQ8051

Revolutionary Quad-Pipelined Ultra High performance 8051 Microcontroller Core



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DQ8051 is an **ultra-high performance, speed-optimized** soft core of a single-chip 8-bit embedded controller, designed to operate with fast (typically on-chip) and slow (off-chip) memories. The core was designed with a special concern about the performance to power-consumption ratio. This ratio is extended by an **advanced power management (PMU)** unit. The DQ8051 softcore is 100% binary-compatible with an industry-standard 8051 8-bit microcontroller. Our powerful 8051 has a built-in, configurable **DoCD-JTAG on-chip debugger**, supporting **Keil µVision development** platform and a standalone DoCD debug software**. Dhrystone 2.1 benchmark program runs from 26.67 to 29.01 times faster than the original 80C51 at the same frequency**. This performance can be also exploited to great advantage in low-power applications, where the core can be clocked over ten times slower than the original implementation, with no performance penalty. The DQ8051 is fully customizable – it is delivered in an exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The DQ8051 is delivered with **a fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each of our 8051 cores has built-in support for DCD's Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger**, which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers, internal and external program memories, all SFRs, including user-defined peripherals.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.
- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

CPU FEATURES

- 100% software compatible with 8051 industry standard
- **Quad-Pipelined** architecture enables to run **29 times faster**, than the original 80C51 at the same frequency
- **Up to 0.27297 VAX MIPS at 100 MHz**
- 24 times faster multiplication
- 12 times faster division
- 2 Data Pointers (DPTR) for faster memory blocks copying
  - Advanced INC & DEC modes
  - Auto-switch of current DPTR
- Up to 256 bytes of internal (on-chip) Data Memory – IDM
- Up to 64k bytes of Program Memory
- Up to 16 MB of external (off-chip) Data Memory – XDM
  - Synchronous interface for up to 64K bytes of (on-chip) fast external Data Memory – (SXDM)
- User programmable Program Memory Wait States solution – for wide range of memories' speed
- User programmable External Data Memory Wait States solution – for wide range of memories' speed
- De-multiplexed Address/Data bus – to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:
The DQ8051 soft core is dedicated for operation with Internal or External Program Memory. Program Memory can be implemented as ROM, RAM or FLASH.

INTERNAL DATA MEMORY:
The DQ8051 can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as synchronous RAM.

EXTERNAL DATA MEMORY:
The DQ8051 soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

SYNCHRONOUS XDM:
The DQ8051 soft core can address up to 64 kB of fast on-chip Synchronous External Data Memory. All reads and writes are executed in one clock cycle.

USER SPECIAL FUNCTION REGISTERS:
Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ8051 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any

address that is not occupied by a core SFR.

WAIT STATES SUPPORT:
The DQ8051 soft core is dedicated to operate with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

PERIPHERALS

- DoCD™ debug unit
  - Processor execution control
    - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoints at
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Hardware watchpoints activated at certain
    - address by any write into memory
    - address by any read from memory
    - address by write into memory a required data
    - address by read from memory a required data
  - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - JTAG Communication interface
- Power Management Unit
  - Power management mode
  - Switchback feature
  - Stop mode
- Extended Interrupt Controller
  - 2 priority levels
  - 2 external interrupt sources
  - 3 interrupt sources from peripherals
- Four 8-bit I/O Ports
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- Two 16-bit timer/counters
  - Timers clocked by internal source
  - Auto reload 8-bit timers
  - Externally gated event counters
- Full-duplex serial port
  - Synchronous mode, fixed baud rate
  - 8-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, variable baud rate

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – It performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages the execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.
External Data Memory Interface – Contains memory access related registers, such as Data Pointer High (DPH), Data Pointer Low (DPL), Data Page Pointer (DPP), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. It also allows applications software to access up to 16 MB of external data memory. The DPP register is used for segments swapping. STRETCH register allows flexible timing management, while accessing different speed system devices, by programming XDATAWR and XDATARD pulse width between 1 and 8 clock periods.
Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by CPU, improving overall performance of application.
Internal Data Memory Interface – Controls an access to the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.
Interrupt Controller – Responsible for the interrupt manage system of external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.
I/O Ports – The block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, and P3.
Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – it's a **real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the **DoCD™** ensures **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when the CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **JTAG interface** and complete set of tools, to communicate and work with the core in a real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

CONFIGURATION

The following parameters of the DQ8051 core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

– Second Data Pointer (DPTR1) – *used/unused*
– DPTR0 decrement – *used/unused*
– DPTR1 decrement – *used/unused*
– Data Pointers auto-switch – *used/unused*
– Data Pointers auto-update – *used/unused*
– Interrupts – *subroutines location*
– Power Management Mode – *used/unused*
– Stop mode – *used/unused*
– Peripherals – *used/unused*
– Synchronous XDM – *size*
– DoCD™ debug unit – *used/unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

One of the most important performance parameter is a real application speed improvement when comparing to the well-known 80C51 architecture. The Dhrystone Benchmark Version 2.1 was used to measure the 80C51 and the DQ8051 core performance. The following table gives a survey about the DQ8051 performance in Dhrystone VAX MIPS per 1 MHz and its improvement vs. 80C51.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DQ8051	0,18527	19,69
DQ8051+DPTRs	0,22369	23,77
DQ8051+DPTRs+SXDM	0,23650	25,13
DQ8051+DPTRs+SXDM+MDU32	0,25053	26,62

The following table gives a survey about the DQ8051 core area in INTEL FPGA Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed	Min area LE/ALM	F_{max}
CYCLONE-III	-6	3 050	60 MHz
CYCLONE-IV GX	-6	3 050	55 MH
STRATIX-III	-2	2 050 LUT	100 MHz
STRATIX-IV	-1	2 050 LUT	90 MHz
STRATIX-V	-2	2 050 LUT	90 MHz

Results given for working system with two DPTRs and 256B IDM, 8kB CODE and 2kB SXDM memories.

DELIVERABLES

- Source code:
  - VERILOG Source Code
  - VERILOG test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation

- HDL core specification
- Datasheet

- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.

– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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