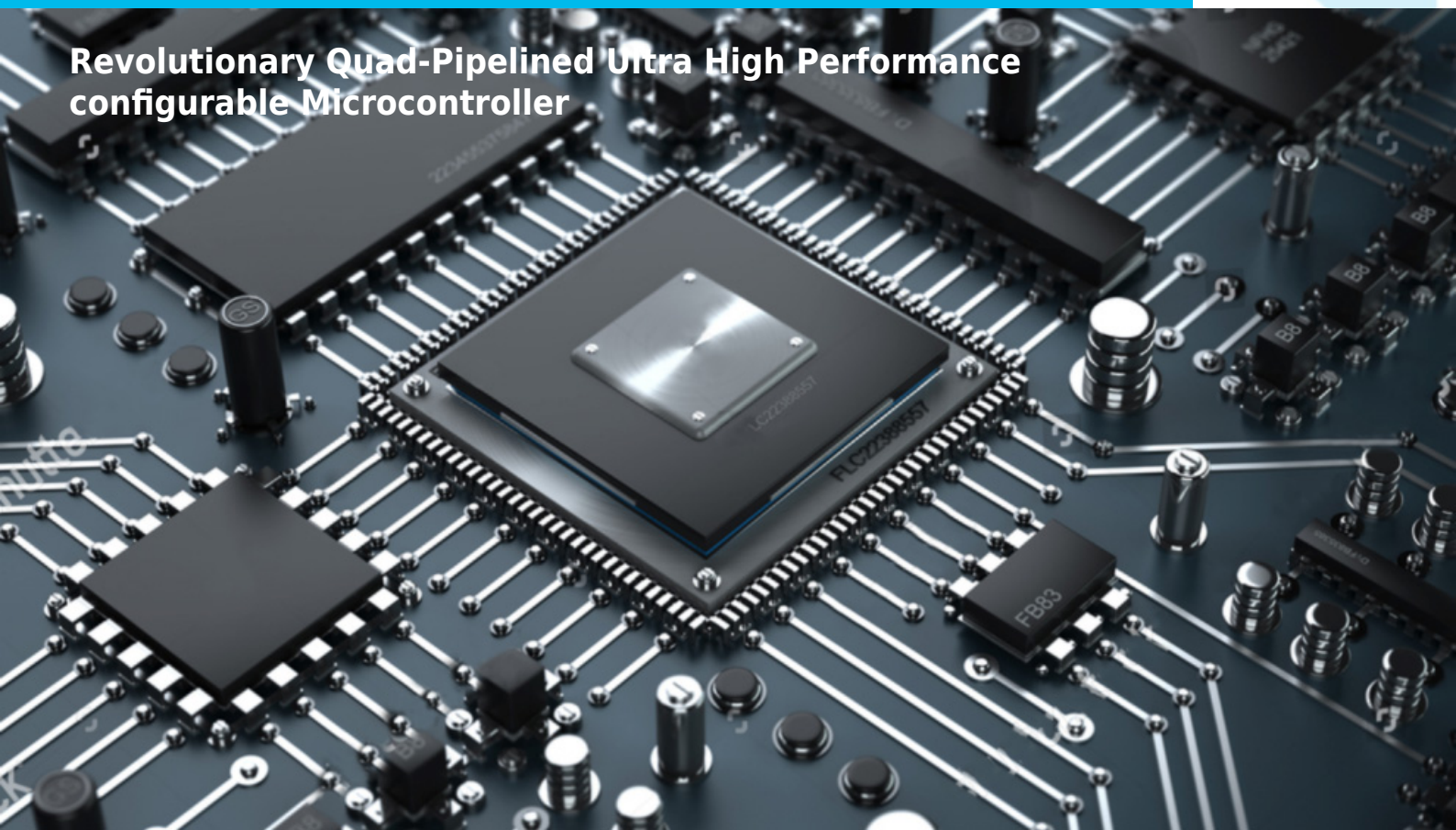
DIGITAL CORE DESIGN

DQ8051XP

Revolutionary Quad-Pipelined Ultra High Performance configurable Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DQ8051XP – ULTRA HIGH PERFORMANCE 8051 SOFT CORE CPU

The **DQ8051XP** is an **ultra-high performance, speed-optimized 8-bit 8051 soft core**, delivering a **dramatic leap forward over classic 8051 microcontrollers**. Designed for modern SoC architectures, it efficiently operates with both **fast on-chip memories and slower off-chip memories**, making it ideal for embedded, industrial, and low-power connected devices.

Performance Without Compromise

- **Up to 29× Faster Than the Original 80C51**
  The DQ8051XP achieves **26.67–29.01× higher Dhrystone 2.1 performance** at the same clock frequency, positioning it among the **fastest 8051-compatible CPUs available worldwide**.

- **Exceptional Performance-to-Power Ratio**
  Thanks to an advanced **Power Management Unit (PMU)**, the core can be clocked **over 10× slower than a traditional 8051** with **no performance loss**, enabling ultra-low-power operation.

100% 8051 Binary Compatibility

The DQ8051XP is **fully binary-compatible with industry-standard 8051 microcontrollers**, allowing seamless reuse of existing software while unlocking a **new level of speed, efficiency, and flexibility**—a true **brave new world for legacy 8051 designs**.

Advanced Debugging with DoCD™

Each DQ8051XP core integrates **DCD's DoCD™ Hardware Debug System**, a powerful, real-time, non-intrusive debugger for complete SoC visibility:

- Halt, run, step into, or skip instructions in real time
- Read/write all registers, SFRs, and internal/external memories
- Debug user-defined peripherals
- Supports **Keil µVision** and standalone **DoCD debug software**
- JTAG-based, configurable on-chip debug interface

Unlike traditional debuggers, **DoCD™ enables full system debugging without disturbing application execution**.

Fully Configurable & SoC-Ready

- **Exact-fit customization** to project requirements
- No cost for unused features or wasted silicon
- Optimized for **single-chip SoC designs**
- Efficient operation with mixed memory architectures

Verification-Ready Delivery

The DQ8051XP is delivered with a **fully automated test bench** and a **complete regression test suite**, ensuring fast, reliable validation at every stage of the **SoC design and verification flow**.

Ideal Applications

- Low-power and battery-powered embedded systems
- Industrial controllers and automation
- IoT and connected devices
- Legacy 8051 system upgrades requiring higher performance

DQ8051XP redefines what an 8051 CPU can deliver—**world-class performance, ultra-low power operation, full compatibility, and professional-grade debugging**, all in a configurable, silicon-efficient IP core designed for modern SoCs.

DCD-SEMI 8051 / 80251 CPU IP CORE

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COMPARISON

Feature / Parameter	DQ8051	DQ8051XP	DQ80251
Architecture Class	8-bit 8051	8-bit 8051 (Extended Performance)	16/32-bit 80251
Binary Compatibility	100% 8051	100% 8051	100% 8051 & 80251
Execution Modes	Binary (8051)	Binary (8051)	Binary (8051) + **SOURCE (80251 native)**
Pipeline Architecture	Advanced pipelined	Enhanced deep pipeline	**Quad-pipelined**
Relative Performance (Dhrystone 2.1)	**26-29×** faster than 80C51	**26-29×** faster than 80C51	**75× faster than 80C51** **6× faster than original 80251**
World-Class Performance Claim	Ultra-fast 8051	**World's fastest 8051 CPU available**	**World's Fastest 8051/80251 CPU**
Instruction Set Efficiency	Optimized 8051	Highly optimized 8051	**Advanced 80251 instruction set**
Code Density Improvement	Improved vs classic 8051	Improved vs classic 8051	**~2× smaller code in SOURCE mode**
Data Width	8-bit	8-bit	16-bit / 32-bit
Addressing Capability	8051 standard	8051 standard	Extended 80251 addressing
Power Management Unit (PMU)	Yes	**Yes (advanced)**	**Yes (advanced)**
Low-Power Operation	Clock scaling supported	**>10× slower clock with no performance loss**	**>50× slower clock with no performance loss**
On-Chip Debug	DoCD™ JTAG	DoCD™ JTAG	**DoCD™ JTAG (advanced)**
Debugger Features	Non-intrusive real-time debug	Non-intrusive real-time debug	Non-intrusive full SoC debug
Keil Toolchain Support	Yes	Yes	**Keil DK251 + DoCD™**
Memory Architecture	On-chip & off-chip	On-chip & off-chip	On-chip & off-chip
Customization Level	High	**Very High**	**Maximum (CPU + instruction model)**
Testbench & Verification	Fully automated	Fully automated	Fully automated
Typical Use Cases	Legacy 8051 replacement	High-performance / low-power 8051 systems	High-end embedded, legacy migration, performance-critical SoCs

QUICK SELECTION GUIDE

If you need...	Choose
Drop-in replacement for classic 8051 with massive speed-up	**DQ8051**
Best performance-to-power ratio in an 8051-compatible design	**DQ8051XP**
A **true next-generation leap beyond 8051**, with 80251 performance	**DQ80251**

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- software in 100% compatible with 8051 industry standard
- **Quad-Pipelined** architecture enables to run **29.01 times faster** , than the original 80C51 at the same frequency
- **Up to 27.297 VAX MIPS at 100 MHz**
- 24 times faster multiplication
- 12 times faster division
- 2 Data Pointers (DPTR) – for faster memory blocks copying
- Advanced INC & DEC modes
- Auto-switch of current DPTR
- Up to 256 bytes of internal (on-chip) Data Memory – IDM
- Up to 64k bytes of Program Memory
- Up to 16 MB of external (off-chip) Data Memory – XDM
- Synchronous interface, for up to 64K bytes of (on-chip) fast external Data Memory – (SXDM)
- User programmable Program Memory Wait States solution, for wide range of memories speed
- User programmable External Data Memory Wait States solution – for wide range of memories speed
- De-multiplexed Address/Data bus, to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:
The DQ8051XP soft core is dedicated for operation with Internal or External Program Memory. Program Memory can be implemented as ROM, RAM or FLASH.

INTERNAL DATA MEMORY:
The DQ8051XP can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as synchronous RAM.

EXTERNAL DATA MEMORY:
The DQ8051XP soft core can address up to 16MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

SYNCHRONOUS XDM:
The DQ8051XP soft core can address up to 64kB of fast on-chip Synchronous External Data Memory. All reads and writes are executed in one clock cycle.

USER SPECIAL FUNCTION REGISTERS:
Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ8051XP design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and

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0xFF, in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:
The DQ8051XP soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

PERIPHERALS

- DoCD™ debug unit
  - Processor execution control
    - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoints at
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Hardware watchpoints activated at a certain
    - address by any write into memory
    - address by any read from memory
    - address by write into memory a required data
    - address by read from memory a required data
  - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - JTAG Communication interface
- Power Management Unit
  - Power management mode
  - Switchback feature
  - Stop mode
- Extended Interrupt Controller
  - 2 priority levels
  - Up to 7 external interrupt sources
  - Up to 8 interrupt sources from peripherals
- Four 8-bit I/O Ports
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- Three 16-bit timer/counters
  - Timers clocked by internal source
  - Auto reload 8/16-bit timers
  - Externally gated event counters
- Two full-duplex serial ports
  - Synchronous mode, fixed baud rate
  - 8-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, variable baud rate
- I2C bus controller – Master
  - 7-bit and 10-bit addressing modes
  - NORMAL, FAST, FAST+, HIGH speeds
  - Multi-master systems supported
  - Clock arbitration and synchronization
  - User defined timings on I2C lines
  - Wide range of system clock frequencies
  - Interrupt generation
- I2C bus controller – Slave
  - NORMAL speed 100 kB/s
  - FAST speed 400 kB/s
  - FAST+ speed 1000 kB/s
  - HIGH speed 3400 kB/s
  - Wide range of system clock frequencies
  - User defined data setup time on I2C lines
  - Interrupt generation
- SPI – Master and Slave Serial Peripheral Interface
  - Supports speeds up ¼ of system clock
    - Mode fault error
    - Write collision error
  - Four transfer formats supported
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
  - Interrupt generation
- Programmable Watchdog Timer
- 16-bit Compare/Capture Unit
  - Events capturing
  - Pulses generation
  - Digital signals generation
  - Gated timers
  - Sophisticated comparator
  - Pulse width modulation
  - Pulse width measuring
- Fixed-Point arithmetic coprocessor
  - Multiplication – 16bit * 16bit
  - Multiplication – 32bit * 32bit
  - Division – 32bit / 32bit
  - Division – 16bit / 16bit
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
  - FADD, FSUB – addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM – compare
  - FCHS – change sign
  - FABS – absolute value
- Floating-Point math coprocessor – IEEE-754 standard single precision real, word and short integers
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS – change sign
  - FABS – absolute value
  - FSIN, FCOS- sine, cosine
  - FTAN, FATAN- tangent, arcs tangent
- And more peripherals

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic

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operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Data Memory Interface – Contains memory access related registers, such as Data Pointer High (DPH), Data Pointer Low (DPL), Data Page Pointer (DPP), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. It also allows applications software to access up to 16MB of external data memory. The DPP register is used for segments swapping. STRETCH register allows flexible timing management, while accessing different speed system devices, by programming XDATAWR and XDATARD pulse width between 1 and 8 clock periods.

Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by CPU, improving overall performance of application.

Internal Data Memory Interface – This interface controls access to internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Controls the access to special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

I/O Ports – This block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, and P3.

Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – A **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. The CODERUN is active, when the CPU is executing an instruction. The DEBUGACS pin is active, when any access is performed by the **DoCD™** debugger. The **DoCD™** system includes **JTAG interface** and complete set of tools, to communicate and work with core in real time debugging. It is built as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

DRTC – Provides Real Time Clock Calendar storing current time in Unix epoch format. The Unix epoch (called also POSIX time, Unix timestamp or Unix time) is the number of seconds that have elapsed since 1st January 1970 midnight UTC/GMT, not counting leap seconds (in ISO 8601: 1970-01-01T00:00:00Z). Many systems store epoch dates as a signed 32-bit integer, which might cause problems on 19th January 2038 (0x7FFFFFFF known as the Year 2038 problem). The DRTC has no such problem since its time is stored as unsigned 32-bit integer allowing correct work until 0xFFFFFFFF which is 07/Feb/2106. Additionally it can be extended to hold later future time.

Floating Point Unit – The FPMU contains floating point arithmetic IEEE-754 compliant instructions (C **float, int, long int** types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm, a full set of trigonometric operations is also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface that allows easy usage and interfacing with user's C/ASM written programs.

MDU32 Multiply Divide Unit – It is a fixed point fast, 16-bit and 32-bit multiplication and division unit. It supports unsigned and 2,s complement signed integer operands. The MDU32 is controlled by dedicated direct memory access module (called DMA). All arguments and result registers are automatically read and written back by internal DMA. This unit has included standard software interface, that allows easy usage and interfacing with user C/ASM written programs. **This module is a modern replacement for older MDU.**

Timers – System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer

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registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Timer 2 – Second system timer module – contains one 16-bit configurable timer: Timer 2 (TH2, TL2); capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it is presented in the system. It can be used as clock source for UART0.

Compare Capture Unit – A compare/capture/reload unit is one of the most powerful peripheral units of the core. It can be used for all kind of digital signal generation and event capturing, such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – The watchdog timer is a 27-bit counter, which is incremented in every system clock period (CLK pin). It performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

UART1 – Universal Asynchronous Receiver and Transmitter module. It is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF1, loads the transmit register and reading SBUF1, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer1.

Master I2C Unit – Incorporates all features required by I2C specification. Supports both 7-bit and 10-bit addressing modes, on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization, letting it to operate in multi-master systems. Built-in timer allows operation from wide range of input frequencies. The timer allows achieving any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed – up to 3400kbs.

Slave I2C Unit – Incorporates all features required by I2C specification. It works as a slave transmitter/receiver, depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400kbs.

SPI Unit – A fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

CONFIGURATION

The following parameters of the DQ8051XP core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

– Second Data Pointer (DPTR1) – *used/unused*
– DPTR0 decrement – *used/unused*
– DPTR1 decrement – *used/unused*
– Data Pointers auto-switch – *used/unused*
– Data Pointers auto-update – *used/unused*
– Interrupts – *subroutines location*
– Timing access protection – *used/unused*
– Power Management Mode – *used/unused*
– Stop mode – *used/unused*
– Peripherals – *used/unused*
– Synchronous XDM – *size*
– DoCD™ debug unit – *used/unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

One of the most important performance parameters is a real application speed improvement compared to the well-known 80C51 architecture. The Dhrystone Benchmark Version 2.1 was used to measure the 80C51 and the DQ8051XP core performance. The following table gives a survey about the DQ8051XP performance in Dhrystone VAX MIPS per 1 MHz and its improvement vs. 80C51.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DQ8051	0,18527	19,69
DQ8051+DPTRs	0,22369	23,77
DQ8051+DPTRs+SXDM	0,23650	25,13
DQ8051+DPTRs+SXDM+MDU32	0,25053	26,62

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The following table gives a survey about the DQ8051XP core area in **LATTICE** Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed	Min area	F_{max}
XP2	-7		91 MHz
ECP2	-7		104 MHz
ECP3	-7		171 MHz
SC	-7		180 MHz

DQ8051XP core area in LATTICE® devices.
Results given for a working system with IDM, CODE and SXDM memories.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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