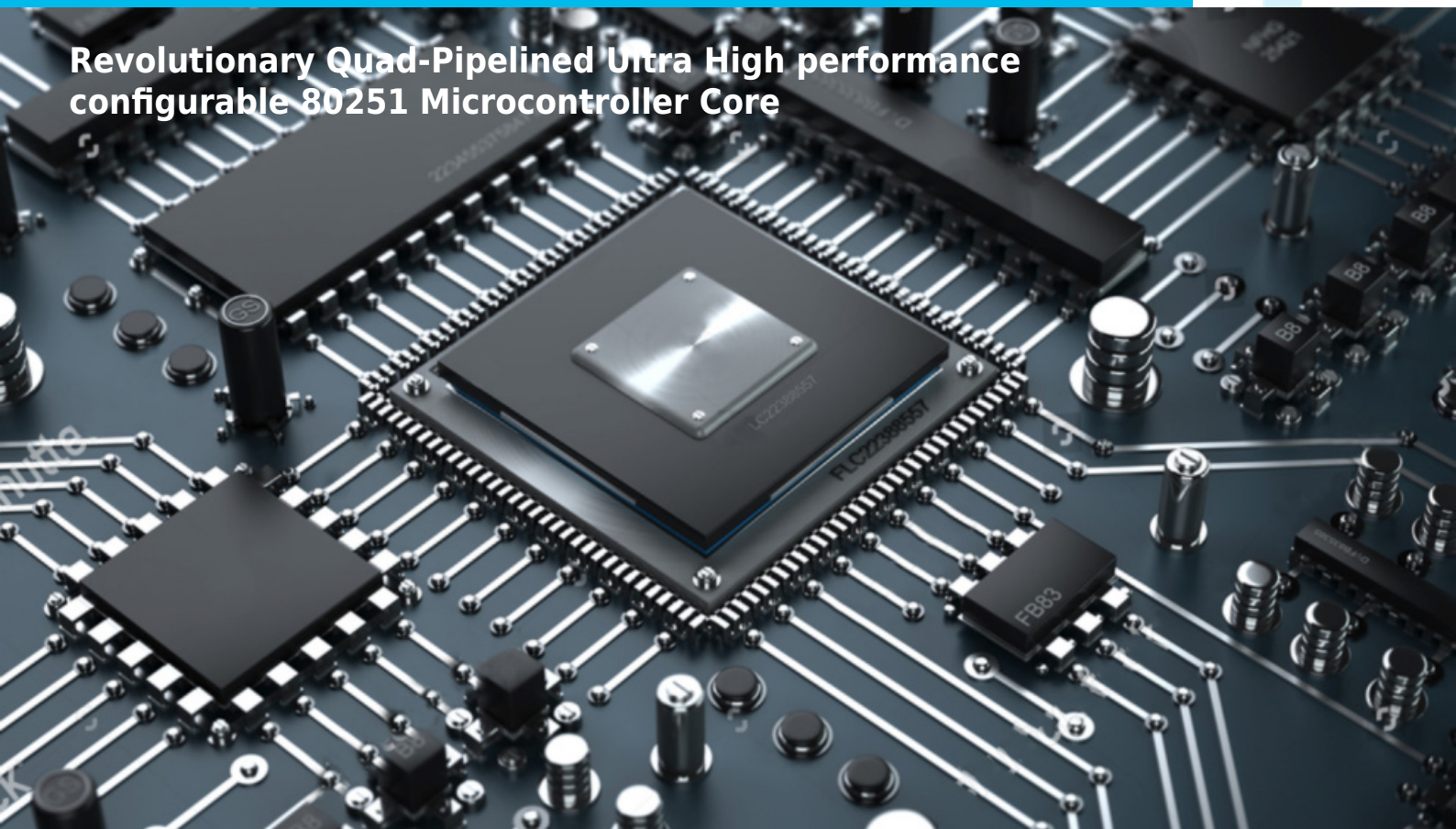


# DQ80251



**Revolutionary Quad-Pipelined Ultra High performance  
configurable 80251 Microcontroller Core**



## COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

## IP CORE OVERVIEW

The DQ80251 is a revolutionary Quad-Pipelined ultra high performance, **speed optimized soft core** of a 16-bit/32-bit embedded microcontroller. The core is **fully configurable** – this allows an easy selection of features and peripherals, in order to create a dedicated system. It was designed with a special concern about the **performance to power consumption ratio**. This ratio is extended by an advanced power management unit – the **PMU**. The DQ80251 utilizes 20 years of DCD's know-how with triumphant 8051 architectures. The core is **100% binary-compatible** with industry-standard 16-bit 80C251 and 8-bit 80C51 microcontrollers. There are two working modes of the DQ80251:

- BINARY (where the original 80C51 compiled code is executed), and
- SOURCE (a native 80C251 mode using all DQ80251 performance).

The DQ80251 has a **built-in, configurable DoCD-JTAG on-chip debugger**, supporting Keil DK251 and a standalone DoCD debug software. Dhrystone 2.1 benchmark program runs over **75 times faster than the original 80C51** and **6 times faster than the original 80C251** at the same frequency. This performance can be also exploited to great advantage in low-power applications, where the core can be clocked over fifty times slower than the original implementation, with no performance penalty. Additionally, the **compiled code size** for the SOURCE mode is **about 2 times smaller** compared to the identical standard 8051 code, due to the higher efficiency of DQ80251 instructions. The DQ80251 is delivered with **fully automated test bench and a complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each of our 80251 cores has built-in support for DCD's Hardware Debug System called DoCD™. It is a real-time hardware debugger that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™ provides non-intrusive debugging of running applications**. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers, internal and external program memories, and all SFRs, including user-defined peripherals.

Watch the DQ80251 presentation on DCD's YouTube:

As Seen On YouTube™

### DESIGN FEATURES:

**ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.**

- **Altera / Intel,**
- **Xilinx / AMD,**
- **Lattice,**
- **Microsemi / Microchip,**  
*and others.*
- **TSMC**
- **UMC**
- **SK Hynix**  
*and others.*

## CPU FEATURES

- 100% binary compatible with industry standard 80C251, implementing BINARY and SOURCE modes
- Single clock period per most of instructions
- **Quad-Pipelined** architecture enables to run **75 times faster** than the original 80C51 and 6 times faster, than the 80C251 at the same frequency
- **Up to 75.08 VAX MIPS ratio**
- Up to 8M bytes of Program Memory
- Up to 32k bytes of internal (on-chip) Data Memory
- Up to 8M bytes of external (off-chip) Data Memory
- **Up to 16 MB of total memory space for CODE and DATA**
- 32k bytes of extended stack space
- User programmable Program Memory Wait States solution – for wide range of memories' speed
- User programmable Extended Data Memory Wait States solution – for wide range of memories' speed
- De-multiplexed Address/Data bus, to allow easy connection to memory
- Full Program Memory writes
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

## DESIGN FEATURES

### PROGRAM MEMORY:

The DQ80251 is dedicated for operation with Internal and External Program Memory up to 8MB of size. It can be configured as synchronous or asynchronous.

### DATA MEMORY:

The DQ80251 can address synchronous Internal Data Memory of up to 32k bytes and up to 8MB of External Data Memory. The External Data Memory interface can be configured as synchronous or asynchronous. XDATA memory (from 8051/

80390) is inside the EDATA space.

#### USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ80251 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner, as core SFRs and may occupy any address which is not occupied by a core SFR.

#### WAIT STATES SUPPORT:

The DQ80251 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and Extended Data memory may assert memory WAIT signals, to hold up CPU activity for required period of time.

## PERIPHERALS

### • DoCD™ debug unit

- Processor execution control
  - Run, Halt
  - Step into instruction
  - Skip instruction
- Read-write all processor contents
  - Program Counter (PC)
  - Program Memory
  - Internal (direct) Data Memory
  - Special Function Registers (SFRs)
  - Extended Data Memory
- Code execution breakpoints
  - up to eight real-time PC breakpoints
  - unlimited number of real-time OP CODE breakpoints
- Hardware execution watchpoints at
  - Internal Data Memory
  - Extended Data Memory
  - Special Function Registers (SFRs)
- Hardware watchpoints activated at a certain
  - address by any write into memory
  - address by any read from memory
  - address by write into memory a required data
  - address by read from memory a required data
- Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
- Automatic adjustment of debug data transfer speed rate between HAD and Silicon
- JTAG Communication interface

### • Power Management Unit

- Power management mode
- Switchback feature
- Stop mode

### • Extended Interrupt Controller

- 4 priority levels
- 7 external interrupt sources (or more)
- Up to 9 interrupt sources from peripherals

### • Four 8-bit I/O Ports

- Bit addressable data direction for each line
- Read/write of single line and 8-bit group

### • Three 16-bit timer/counters

- Timers clocked by internal source
- Auto reload 8/16-bit timers
- Externally gated event counters

### • Two Full-duplex serial port

- Synchronous mode, fixed baud rate

- 8-bit asynchronous mode, fixed baud rate
- 9-bit asynchronous mode, fixed baud rate
- 9-bit asynchronous mode, variable baud rate

### • I2C bus controller - Master

- 7-bit and 10-bit addressing modes
- NORMAL, FAST, FAST+, HIGH speeds
- Multi-master systems supported
- Clock arbitration and synchronization
- User defined timings on I2C lines
- Wide range of system clock frequencies
- Interrupt generation

### • I2C bus controller - Slave

- NORMAL speed 100 kB/s
- FAST speed 400 kB/s
- FAST+ speed 1000 kB/s
- HIGH speed 3400 kB/s
- Wide range of system clock frequencies
- Interrupt generation

### • SPI - Master and Slave Serial Peripheral Interface

- Supports speeds up  $\frac{1}{4}$  of system clock
  - Mode fault error
  - Write collision error
- Four transfer formats supported
- System errors detection
- Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
- Interrupt generation

### • Programmable Watchdog Timer

### • 16-bit Compare/Capture Unit

- Events capturing
- Pulses generation
- Digital signals generation
- Gated timers
- Sophisticated comparator
- Pulse width modulation
- Pulse width measuring

### • Fixed-Point arithmetic coprocessor

- Multiplication – 32bit \* 32bit
- Division – 32bit / 32bit

### • Floating-Point arithmetic coprocessor IEEE-754 standard single precision

- FADD, FSUB – addition, subtraction
- FMUL, FDIV- multiplication, division
- FSQRT- square root
- FUCOM – compare
- FCHS – change sign
- FABS – absolute value

### • Floating-Point math coprocessor - IEEE-754 standard single precision real word and short integers

- FADD, FSUB- addition, subtraction
- FMUL, FDIV- multiplication, division
- FSQRT- square root
- FUCOM- compare
- FCHS – change sign
- FABS – absolute value
- FSIN, FCOS- sine, cosine
- FTAN, FATAN- tangent, arcs tangent

### • DUSB2 - USB 2.0 device controller

### • DMAC - Ethernet controller

### • And more peripherals

## UNITS SUMMARY

**ALU** - 16/32-bit Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW, PSW1), (B) registers and related logic, such as arithmetic unit, logic unit, multiplier and divider.

**REGFILE** - Contains complete set of 80251 dedicated: 8-bit {R0, R1, ..., R15} registers, 16-bit {WR0, WR2, ..., WR30} and 32-bit {DR0, DR4, ..., DR28, DR56, DR60} registers.

**Opcode Decoder** - Performs an opcode decoding instruction and control functions for all other blocks.

**Control Unit** - Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.

**Program Memory Interface** - Contains Program Counter (PC) and related logic. It performs instructions code fetching. Program Memory (CODE) can be also written. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States and allows core to work with different speed program memories. It works with synchronous or asynchronous memories.

**EDATA Memory Interface** - Contains memory access related registers. It performs the Extended Data Memory (EDATA) addressing and data transfers. EDATA read/write cycle length can be programmed by user. EDATA covers also XDATA space from 80C51. This feature is called EDATA Memory Wait States and allows core to work with different speed memories. It is fully configurable. It works with synchronous or asynchronous memories.

**Internal Data Memory Interface** - Internal Data Memory interface controls access into the whole 32kB of IDATA memory. It contains 16-bit Stack Pointer (SP) register and related logic. It is fully configurable from 1 kB to 32 kB.

**SFRs Interface** - Special Function Registers interface controls access to the special registers. It contains standard and user defined registers and related logic. All SFR registers are bit addressable. User defined external devices, can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

**Interrupt Controller** - Four Levels interrupt control module is responsible for the interrupt manage system, for external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IPH, IPL) and (TCON) registers. Its upgraded version can be extended by extra user's dedicated interrupt sources. Interrupt vectors locations and spacing are fully configurable.

**Timers** - System timers module. Contains two 16bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

**Ports** - Block contains 8051 general purpose I/O ports. Each of ports pin can be read/write as a single bit or as an 8-bit bus P0, P1, P2, P3.

**Power Management Unit** - contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It's highly desirable, when microcontroller is planned to be used in portable and power critical applications.

**DoCD™ Debug Unit** - a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external data, program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, REGFILE and also on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins - CODERUN and DEBUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by **DoCD™** debugger. The **DoCD™** system includes JTAG interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

**DRTC** - provides Real Time Clock Calendar storing current time in Unix epoch format. The Unix epoch (called also POSIX time, Unix timestamp or Unix time) is the number of seconds that have elapsed since 1st January 1970 midnight UTC/GMT, not counting leap seconds (in ISO 8601: 1970-01-01T00:00:00Z). Many systems store epoch dates as a signed 32-bit integer, which might cause problems on 19th January 2038 (0x7FFFFFFF known as the Year 2038 problem). The DRTC has no such problem since its time is stored as unsigned 32-bit integer allowing correct work until 0xFFFFFFFF which is 07/Feb/2106. Additionally it can be extended to hold later future time.

**Floating Point Unit** - FPMU contains floating point arithmetic IEEE-754 compliant instructions (**C float, int, long int** types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm, a full set of trigonometric operations is also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit has included standard software interface that allows easy usage and interfacing with user's C/ASM written programs.

**MDU32 Multiply Divide Unit** - It is a fixed point fast, 16-bit and 32-bit multiplication and division unit. It supports unsigned and 2's complement signed integer operands. The MDU32 is controlled by dedicated direct memory access module (called DMA). All arguments and result registers are

automatically read and written back by internal DMA. This unit has included standard software interface, that allows easy usage and interfacing with user C/ASM written programs.

**Timer 2** - Second system timer module - contains one 16-bit configurable timer: Timer 2 (TH2, TL2); capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit if it is presented in the system. It can be used as clock source for UART0.

**Compare Capture Unit** - The compare/ capture/reload unit is one of the most powerful peripheral units of the core. It can be used for all kind of digital signal generation and event capturing, such as pulse generation, pulse width modulation, measurements etc.

**Watchdog Timer** - The watchdog timer is a 27-bit counter, which is incremented in every system clock period (CLK pin). It performs system protection against software upsets.

**UART0** - Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of the second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. It works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2 (if present in system).

**UART1** - Universal Asynchronous Receiver and Transmitter module. It is full duplex (it can transmit and receive concurrently). It includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF1, loads the transmit register and reading SBUF1, reads a physically separate receive register. It works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer1.

**Master I2C Unit** - The Master I2C Bus Controller core incorporates all features required by I2C specification. It supports both 7-bit and 10-bit addressing modes, on the I2C bus. It works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization, letting it to operate in multi-master systems. Built-in timer allows operation from wide range of the input frequencies. The timer allows achieving any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed - up to 3400kbs.

**Slave I2C Unit** - The Slave I2C bus controller core incorporates all features required by I2C specification. It works as a slave transmitter/receiver, depending on working mode determined by a master device. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400kbs.

**SPI Unit** - It's a fully configurable master/slave Serial Peripheral Interface, which allows the user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices.

It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of information on two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

## CONFIGURATION

The following parameters of the DQ80251 core can be easily adjusted to requirements of a dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Program Memory Size - *64kB - 8MB*
- Internal Data Memory size - *1kB - 32kB*
- Extended Data Memory size - *1kB - 8MB*
- Program Memory Interface - *synchronous / asynchronous*
- Data Memory Interface - *synchronous / asynchronous*
- Interrupts - *subroutines location*
- Power Management Mode - *used / unused*
- Stop mode - *used / unused*
- DoCD™ debug unit - *enabled with selected features / disabled*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate parameters in the package configuration file.

## DATA MEMORY

The DQ80251 has up to 32k bytes of internal data memory (IDATA) and up to 8MB of extended data memory (EDATA). The lower internal RAM consists of four register banks, with eight registers each. The current bank is selected by a PSW register. A bit addressable segment is mapped in a range from 0x20 to 0xFF and covers part of an internal RAM and all SFR area. With the **16-, 24-bit direct or indirect** addressing mode, 0x80 to 0xFF range of the internal memory is addressed. With the **8-bit direct** addressing mode, the range from 0x80 to 0xFF SFR memory area is accessed. An extended RAM space begins just after end of an Internal RAM memory chip. For example, if the Internal RAM has 1kB size, then the Extended RAM starts at 1 kB address.

## PROGRAM CODE SPACE

Program memory space begins at 0x800000 address and ends at 0xFFFFFFF address. It gives 8MB of code memory. The 64kB memory area, ranged from 0xFF0000 to 0xFFFFFFF, is intended for the MCU51 compatible code. After each reset the CPU starts execution in the program memory at 0xFF0000 location. Each interrupt has its own start address for its service routine. The interrupt vectors are also mapped, starting at 0xFF0000 location.

## PERFORMANCE

To provide you with the most accurate and detailed insights about the Lattice performance, we encourage you to get in touch with us directly.

Please feel free to contact us at [info@dcd.pl](mailto:info@dcd.pl). Our dedicated team will be more than happy to assist you with any inquiries you may have.

## DELIVERABLES

- Source code:
  - VERILOG Source Code
  - VERILOG test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project

- Technical documentation
  - HDL core specification
  - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

## LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.

- **Multi-Site license option** - dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- VHDL or Verilog RTL synthesizable source code (called HDL Source code)

- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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