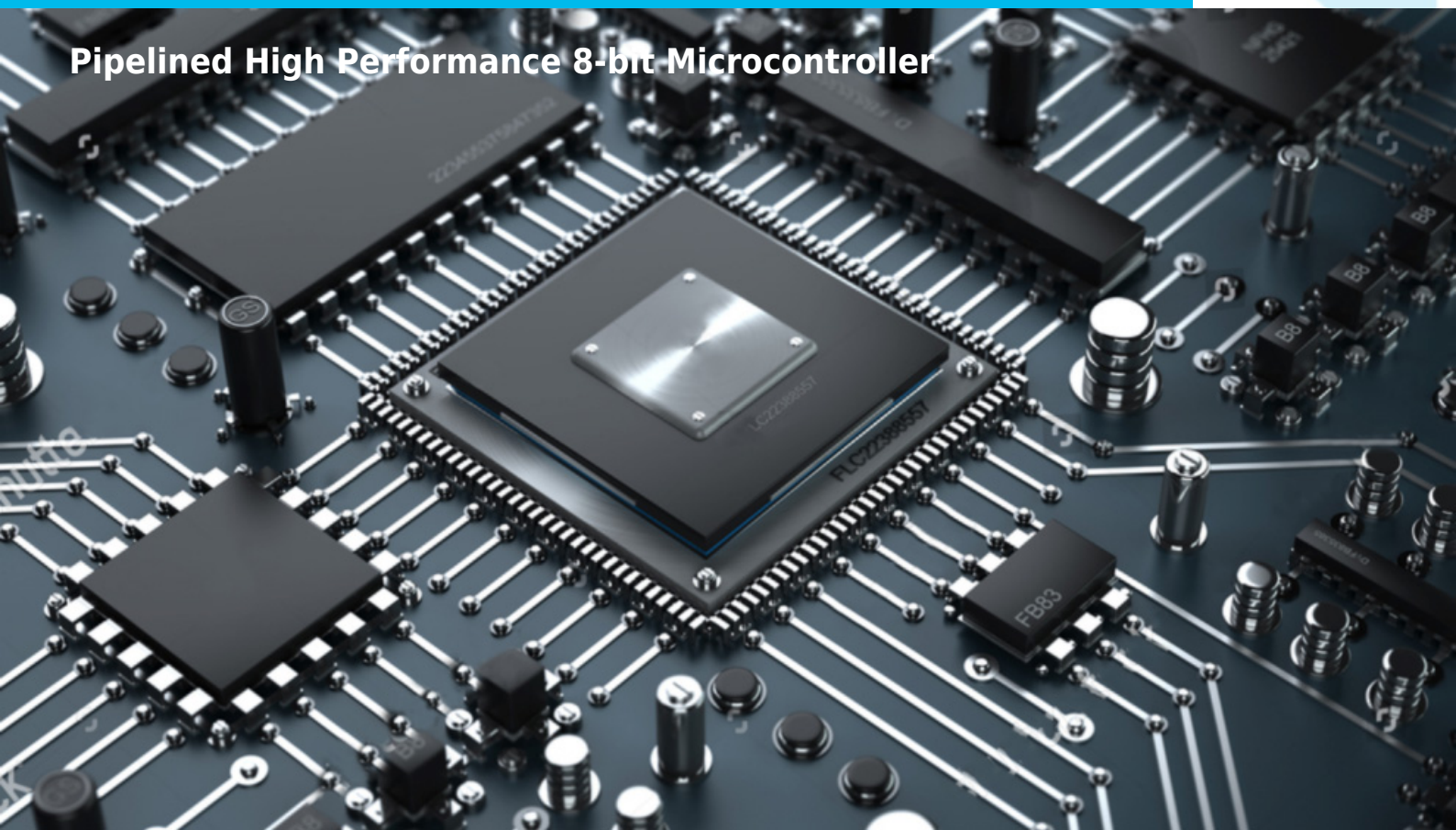
DIGITAL CORE DESIGN

DP8051CPU

Pipelined High Performance 8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DP8051 CPU - ULTRA-HIGH-PERFORMANCE 8051-COMPATIBLE 8-BIT CPU IP CORE

The **DP8051CPU** is an **ultra-high-performance, speed-optimized 8-bit soft microcontroller IP core**, designed for **single-chip SoC implementations** that demand **maximum execution efficiency, low power consumption, and full 8051 software compatibility**.

Engineered to operate with both **fast on-chip memories** and **slower off-chip memory devices**, DP8051CPU achieves an industry-leading **performance-to-power-consumption ratio**, further enhanced by an integrated **Power Management Unit (PMU)**. This makes it an ideal choice for **performance-critical and energy-constrained embedded systems**.

100% 8051 BINARY COMPATIBILITY

DP8051CPU is **fully binary-compatible with industry-standard 8051 microcontrollers**, allowing seamless reuse of **existing firmware, toolchains, compilers, and software libraries**. Legacy 8051 applications can be migrated to **modern ASIC or FPGA platforms** without code changes, while achieving **order-of-magnitude performance improvements**.

FLEXIBLE SOC ARCHITECTURES

To support diverse system requirements, DP8051CPU is available in two architectural configurations:

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- **Harvard architecture** – separate internal program and data buses for maximum throughput
- **von Neumann architecture** – shared program and external data bus for simplified system integration

This flexibility enables SoC designers to optimize **area, memory topology, and performance** based on application needs.

PIPELINED RISC ARCHITECTURE WITH RECORD-CLASS PERFORMANCE

DP8051CPU is built on a **pipelined RISC microarchitecture**, delivering **exceptional performance within the 8-bit MCU class**:

- **120–300 MIPS**, depending on configuration and target frequency
- **Dhrystone 2.1 performance**: **11.46×–15.55× faster** than the original **80C51** at the same clock frequency
- Benchmarked using the **same C compiler and identical compiler settings**, ensuring fair and reproducible results

This high execution efficiency enables **aggressive clock reduction** in low-power designs. DP8051CPU can be clocked **more than 10× slower** than classic 8051 implementations while delivering equivalent system-level performance — dramatically reducing power consumption, thermal output, and EMI.

ADVANCED POWER MANAGEMENT FOR ENERGY-EFFICIENT DESIGNS

The integrated **PMU (Power Management Unit)** allows:

- Dynamic clock and power scaling
- Optimized performance-per-watt operation
- Reduced power dissipation in always-on systems
- Extended battery life in portable and IoT devices

These features make DP8051CPU particularly well suited for **battery-powered, duty-cycled, and ultra-low-energy SoCs**.

SOC-READY VERIFICATION AND NON-INTRUSIVE DEBUGGING

DP8051CPU is delivered with a **fully automated testbench and a complete regression test suite**, enabling **fast IP validation and smooth integration** throughout the SoC design flow.

Each DP8051CPU core includes built-in support for **DoCD™ (Digital Core Design on-Chip Debugger)** — a proprietary **real-time hardware debugging system** that provides **full visibility into a running SoC without disturbing application execution**.

DoCD™ Debug Capabilities

- Run, halt, single-step, step-over, and instruction skipping
- Read/write access to **all CPU registers**, **SFRs**, and **user-defined peripherals**
- Full access to **internal and external program and data memories**
- **True non-intrusive debugging** for real-time embedded applications

KEY BENEFITS FOR DESIGN ENGINEERS

- Industry-leading **8051-compatible CPU IP**
- **Up to 300 MIPS** in an 8-bit architecture
- **11–15× faster** than classic 80C51 at equal clock
- Advanced **PMU for low-power SoCs**
- Harvard or von Neumann architecture options
- Fully synthesizable **ASIC & FPGA-ready soft IP**
- **Non-intrusive, system-wide hardware debugging**
- Complete verification environment included

TARGET APPLICATIONS

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Industrial

- Industrial controllers and I/O subsystems
- Motor control and automation SoCs
- Long-lifecycle embedded platforms

Automotive

- Body electronics and comfort modules
- Automotive monitoring and control units
- Mixed-signal automotive ASICs

IoT & Edge

- Smart sensors and meters
- Battery-powered IoT nodes
- Edge controllers and gateways

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

CPU FEATURES

- software is 100% compatible with 8051 industry standard
- Pipelined RISC architecture enables to run 15.55 times faster, than the original 80C51 at the same frequency
- Up to 16,632 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64 kB of internal (on-chip) or external (off-chip) Program Memory
- Up to 8MB linear code space (in 80390 mode)
- Up to 16 MB of external (off-chip) Data Memory
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- De-multiplexed Address/Data bus to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP8051CPU soft core is dedicated for operation with Internal and External Program Memory. Internal Program Memory can be implemented as:

– ROM located in address range between 0x0000 ¸ (ROM_{size}-1)
– RAM located in address range between (RAM_{size}-1) ¸ 0xFFFF

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ¸ RAM_{size}.

INTERNAL DATA MEMORY:

The DP8051CPU can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented as Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:

The DP8051CPU soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP8051CPU design. ESFRs are memory mapped into Direct Memory, between addresses 0x80 and 0xFF, in the same manner, as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:

The DP8051CPU soft core is designed to be used with wide range of Program and Data memories. Slow Program and External Data memory, may assert a memory Wait signal, to hold up CPU activity.

PERIPHERALS

- DoCD™ debug unit
  - Processor execution control
    - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)

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    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoints at
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Hardware watchpoints activated at certain:
    - address by any write into memory
    - address by any read from memory
    - address by required data write into memory
    - address by required data read from memory
  - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- Power Management Unit
  - Power management mode
  - Switchback feature
  - Stop mode
- Interrupt Controller
  - 2 priority levels
  - 2 external interrupt sources

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and it manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.
External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core, to work with different speed program memories.
Synchronous eXternal Data Memory (SXDM) Interface – Contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used, to store large variables frequently accessed by CPU, improving overall performance of application.
Internal Data Memory Interface – Controls access into the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.
Interrupt Controller – This module is responsible for the interrupt manage system of the external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.
Power Management Unit – PMU contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It is highly desirable, when microcontroller is planned to be used in portable and power critical applications.
DoCD™ Debug Unit – A **real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS indicate the state of the debugger and CPU. The CODERUN is active, when the CPU is executing an instruction. The DEBUGACS pin is active, when any access is performed by the **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with the core in real time debugging. It is built as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

CONFIGURATION

The following parameters of the DP8051CPU core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.
– Internal Program Memory type: *synchronous/asynchronous*
– Internal Program ROM Memory size: *0 – 64kB*
– Internal Program RAM Memory size: *0 – 64kB*
– Internal Program Memory fixed size: *true/false*

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– Interrupts: *subroutines location*
– Power Management Mode: *used/unused*
– Stop mode: *used/unused*
– DoCD™ debug unit: *used/unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** Programmable Logic Devices after Place & Route (all CPU features and peripherals included):

Technology /optimization	Speed grade	Area [gates]	F_{max}
0.25u area	typical	6 050	100 MHz
0.25u speed	typical	7 600	250 MHz
0.18u area	typical	5 730	100 MHz
0.18u speed	typical	6 900	300 MHz

Core performance in ASIC devices – results given for working system with IDATA, CODE and XDATA memories. The DoCD debugger increases the core size by about 2 100 gates.

For the user, the most important factor is an application speed improvement. The most commonly used arithmetic functions and their improvements are shown in the table below. An improvement was computed as {80C51 clock periods} divided by {DP8051CPU clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the Core performance. The following table shows the DP8051 performance in VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP8051	0,10787	11,46
DP8051+DPTRs	0,13722	14,58
DP8051+DPTRs+SXDM	0,14457	15,36
DP8051+DPTRs+SXDM+MDU32	0,14632	15,55

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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