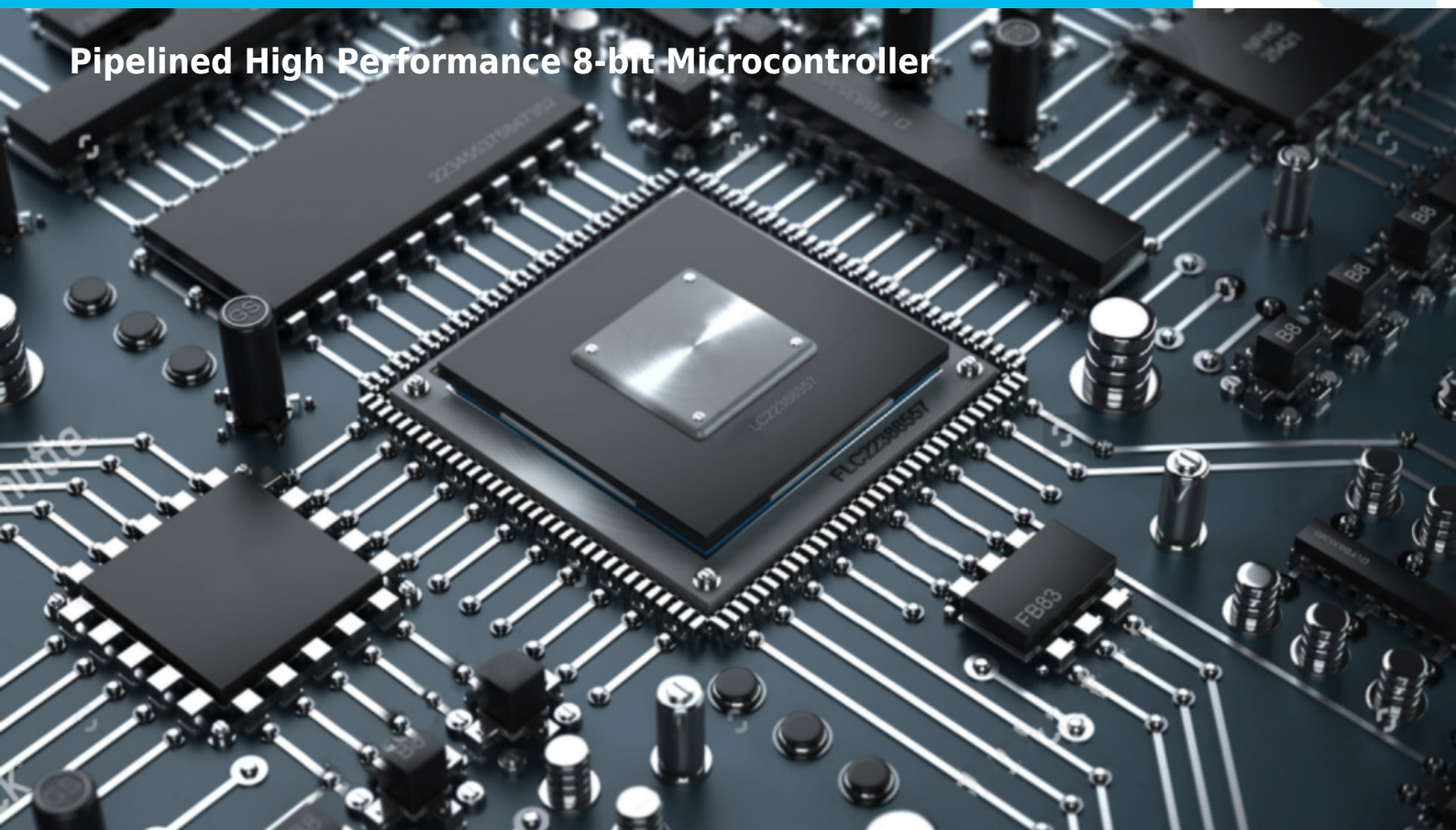
DIGITAL CORE DESIGN

DP8051XP

Pipelined High Performance 8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DP8051XP is an **ultra high performance**, **speed optimized** soft core, of a single-chip, 8-bit embedded controller, intended to operate with fast (typically on-chip) and slow (off-chip) memories. The core was designed with a special concern about performance to power consumption ratio. This ratio is extended by the **PMU** – an **advanced power management unit**.
The DP8051XP soft core is 100% binary-compatible with industry standard 8051 8-bit microcontroller. There are two configurations of the DP8051XP:

- Harvard, where internal data and program buses are separated, and
- von Neumann, with common program and external data bus

The DP8051XP has a Pipelined RISC architecture and executes 120-300 million instructions per second. **Dhrystone 2.1 benchmark program runs from 11.46 to 15.55 times faster than the original 80C51 at the same frequency.** The same C compiler was used for benchmarking of the core vs 80C51 with the same settings. This performance can be also exploited to great advantage in low power applications, where the core can be clocked over ten times slower than the original implementation, without performance depletion. The DP8051XP is delivered with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow. Each of DCD's 8051 Cores has a built-in support for a proprietary Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger**, which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals.

CPU FEATURES

- Software in 100% compatible with 8051 industry standard
- Pipelined RISC architecture enables to run 15.55 times faster, than the original 80C51 at the same frequency
- Up to 14.632 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster division
- 2 Data Pointers (DPTR) – for faster memory blocks copying
- Advanced INC & DEC modes
- Auto-switch of current DPTR
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64 kB of internal (on-chip) or external (off-chip) Program Memory
- Up to 8MB linear code space (in 80390 mode)
- Up to 16 MB of external (off-chip) Data Memory
- Synchronous eXternal Data Memory (SXDM) Interface
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- De-multiplexed Address/Data bus – to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP8051XP soft core is dedicated for operation with Internal and External Program Memory. Internal Program Memory can be implemented as:

– ROM located in address range between 0x0000 ¸ (ROM_{size}-1)
– RAM located in address range between (RAM_{size}-1) ¸ 0xFFFF

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ¸ RAM_{size}.

INTERNAL DATA MEMORY:

The DP8051XP can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:

The DP8051XP soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DP8051XP design. ESFRs are memory mapped into Direct Memory, between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:

The DP8051XP soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and

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External Data memory may assert a memory Wait signal, to hold up CPU activity.

PERIPHERALS

- **DoCD™ debug unit**
  - Processor execution control
    - Run, Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoints at
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Hardware watchpoints activated at certain:
    - address by any write into memory
    - address by any read from memory
    - address by write into memory required data
    - address by read from memory required data
  - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- **Power Management Unit**
  - Power management mode
  - Switchback feature
  - Stop mode
- **Extended Interrupt Controller**
  - 2 priority levels
  - Up to 7 external interrupt sources
  - Up to 8 interrupt sources from peripherals
- **Four 8-bit I/O Ports**
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- **Three 16-bit timer/counters**
  - Timers clocked by internal source
  - Auto reload 8/16-bit timers
  - Externally gated event counters
- **Two full-duplex serial ports**
  - Synchronous mode, fixed baud rate
  - 8-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, variable baud rate
- **I2C bus controller – Master**
  - 7-bit and 10-bit addressing modes
  - NORMAL, FAST, FAST+, HIGH speeds
  - Multi-master systems supported
  - Clock arbitration and synchronization
  - User defined timings on I2C lines
  - Wide range of system clock frequencies
  - Interrupt generation
- **I2C bus controller – Slave**
  - NORMAL speed 100 kB/s
  - FAST speed 400 kB/s
  - FAST+ speed 1000 kB/s
  - HIGH speed 3400 kB/s
  - Wide range of system clock frequencies
  - User defined data setup time on I2C lines
  - Interrupt generation
- **SPI – Master and Slave Serial Peripheral Interface**
  - Supports speeds up ¼ of system clock
    - Mode fault error
    - Write collision error
  - Four transfer formats supported
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
  - Interrupt generation
- **Programmable Watchdog Timer**
- **16-bit Compare/Capture Unit**
  - Events capturing
  - Pulses generation
  - Digital signals generation
  - Gated timers
  - Sophisticated comparator
  - Pulse width modulation
  - Pulse width measuring
- **Fixed-Point arithmetic coprocessor**
  - Multiplication – 16bit * 16bit
  - Multiplication – 32bit * 32bit
  - Division – 32bit / 32bit
  - Division – 16bit / 16bit
- **Floating-Point arithmetic coprocessor IEEE-754 standard single precision**
  - FADD, FSUB – addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM – compare
  - FCHS – change sign
  - FABS – absolute value
- **Floating-Point math coprocessor – IEEE-754 standard single precision real, word and short integers**
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS – change sign
  - FABS – absolute value
  - FSIN, FCOS- sine, cosine
  - FTAN, FATAN- tangent, arcs tangent
- **And more peripherals**

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an opcode decoding instruction

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and control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. Connected to Opcode Decoder, manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. Performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C and DoCD™ module.

External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. Performs external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core to work with different speed program memories.

Synchronous eXternal Data Memory Interface – Contains XDATA memory access related logic, allowing fast access to synchronous memory devices. Performs the external Data Memory addressing and data transfers. This memory can be used to store large variables frequently accessed by the CPU, improving overall performance of an application.

Internal Data Memory Interface – Controls access into the internal memory of size up to 256 bytes. Contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. Contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) by using all direct addressing mode instructions.

Interrupt Controller – Responsible for the interrupt manage system for the external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP), Extended Interrupt Enable (EIE), Extended Interrupt priority (EIP) and (TCON) registers.

I/O Ports – Contains 8051's general purpose I/O ports. Each of port's pin can be read/written as a single bit or as an 8-bit bus called P0, P1, P2, and P3.

Power Management Unit – Contains advanced power saving mechanisms with a switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in a full speed mode, if enabled. It is highly desirable when the microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – A **real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the **DoCD™** ensures **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without a pattern. Two additional pins: CODERUN and DEBUGACS indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by the **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with core in real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

Floating Point Unit – FPMU contains floating arithmetic point xIEEE-754, compliant instructions (C **float, int, long int** types supported). It is used to execute single precision floating point operations such as: addition, subtraction, multiplication, division, square root, comparison absolute value of number and change of sign. Basing on specialized CORDIC algorithm, full set of trigonometric operations is also allowed: sine, cosine, tangent, arctangent. It also has built-in integer to floating point and vice versa conversion instructions. The FPU supports single precision real numbers, 16-bit and 32-bit signed integers. This unit incorporates standard software interface which enables easy usage and interfacing with user's C/ASM written programs.

MDU32 Multiply Divide Unit – A fixed point, fast 16-bit and 32-bit multiplication and division unit. Supports unsigned and 2's complement signed integer operands. The MDU32 is controlled by dedicated direct memory access module (called DMA). All arguments and result registers are automatically read and written back by internal DMA. This unit incorporates standard software interface which allows easy usage and interfacing with user C/ASM written programs. **This module is a modern replacement for older MDU.**

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

Timer 2 – Second system timer module contains one 16-bit configurable timer: Timer 2 (TH2, TL2), capture registers (RLDH, RLDL) and Timer 2 Mode (T2MOD) register. It can work as a 16-bit timer / counter, 16-bit auto-reload timer / counter. It also supports compare capture unit (if present in the system). It can be used as clock source for UART0.

Compare Capture Unit – One of the most powerful peripheral units of the core. It can be used for all kind of digital signal generation and event capturing, such as pulse generation, pulse width modulation, measurements etc.

Watchdog Timer – A 27-bit counter incremented in every system clock period (CLK pin). Performs system protection against software upsets.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means it can transmit and receive concurrently. Includes Serial Configuration register (SCON),

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serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous mode. UART0 can be synchronized by Timer 1 or Timer 2 (if present in the system).

UART1 – Universal Asynchronous Receiver and Transmitter module is full duplex – it can transmit and receive concurrently. Includes Serial Configuration register (SCON1), serial receiver and transmitter buffer (SBUF1) registers. Its receiver is double-buffered, which means, it can commence reception of a second byte before the previously received byte has been read from the receive register. Writing to SBUF1, loads the transmit register and reading SBUF1, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART1 is synchronized by Timer 1.

Master I2C Unit – I2C bus controller is a Master module. Incorporates all features required by the I2C specification. Supports both 7-bit and 10-bit addressing modes on the I2C bus and works as a master transmitter and receiver. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master systems. Built-in timer enables operation within a wide range of input frequencies. The timer allows achieving any non-standard clock frequency. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400 kB/s.

Slave I2C Unit – I2C bus controller is a Slave module. Incorporates all features required by the I2C specification. Works as a slave transmitter/receiver, depending on a working mode determined by the master device. The I2C controller supports all transmission modes: Standard, Fast, Fast+ and High Speed up to 3400 kB/s.

SPI Unit – A fully configurable master/slave Serial Peripheral Interface which allows the user to configure polarity and phase of serial clock signal SCK. Allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communication in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data is simultaneously transmitted and received. The SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The data transfer rate up to CLK/4. Clock control logic allows selecting clock polarity and choosing the two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, the software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register, while the transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers, if more than one SPI device simultaneously attempts to become a bus master.

CONFIGURATION

The following parameters of the DP8051XP core can be easily adjusted to requirements of a dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

– Internal Program Memory type: *synchronous / asynchronous*
– Internal Program ROM Memory size: *0 – 64kB*
– Internal Program RAM Memory size: *0 – 64kB*
– Internal Program RAM Memory size: *0 – 64kB*
– Internal Program Memory fixed size: *true / false*
– Second Data Pointer (DPTR1): *used / unused*
– DPTR0 decrement: *used / unused*
– DPTR1 decrement: *used / unused*
– Data Pointers auto-switch: *used / unused*
– Interrupts: *subroutines location*
– Timing access protection: *used / unused*
– Power Management Mode: *used / unused*
– Stop mode: *used / unused*
– DoCD™ debug unit: *used / unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following table gives a survey about the Core area and performance in ASIC Devices (CPU features and peripherals included):

Technology /optimization	Speed grade	Area [gates]	F_{max}
0.25u area	typical	18 950	100 MHz
0.25u speed	typical	23 900	220 MHz
0.18u area	typical	**17 565**	100 MHz
0.18u speed	typical	21 000	280 MHz

Core performance in ASIC devices – results given for working system with IDATA, CODE and XDATA memories. DoCD debugger increases core size about 2100 gates.

For the user, the most important factor is an application speed improvement. The most commonly used arithmetic functions and their improvement are shown in the following table. The improvement was computed as {80C51 clock periods} divided by {DP8051XP clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**

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8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the core performance. The following table shows the DP8051XP performance in VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP8051	0,10787	11,46
DP8051+DPTRs	0,13722	14,58
DP8051+DPTRs+SXDM	0,14457	15,36
DP8051+DPTRs+SXDM+MDU32	0,14632	15,55

The area utilized by each unit of the DP8051XP core in vendor specific technologies is summarized in the following table.

Component	Area [Gates]
CPU*	5 600
DPTR1 register	200
DPTR0 decrement	100
DPTR1 decrement	100
DPTR0 & DPTR1 auto-switch	50
SXDM	40
Timed Access protection	20
Interrupt Controller	100
INT2-INT6	225
Power Management Unit	90
I/O ports	270
Timers	880
Timer 2	690
UART0	750
UART1	870
Master I2C Unit	1 350
Slave I2C Unit	640
SPI Unit	910
Compare Capture Unit	1 040
Watchdog Timer	480
Multiply Divide Unit 32	3 160
Total area	**17 565**

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface – results given for working system with IDATA, CODE and XDATA memories.

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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