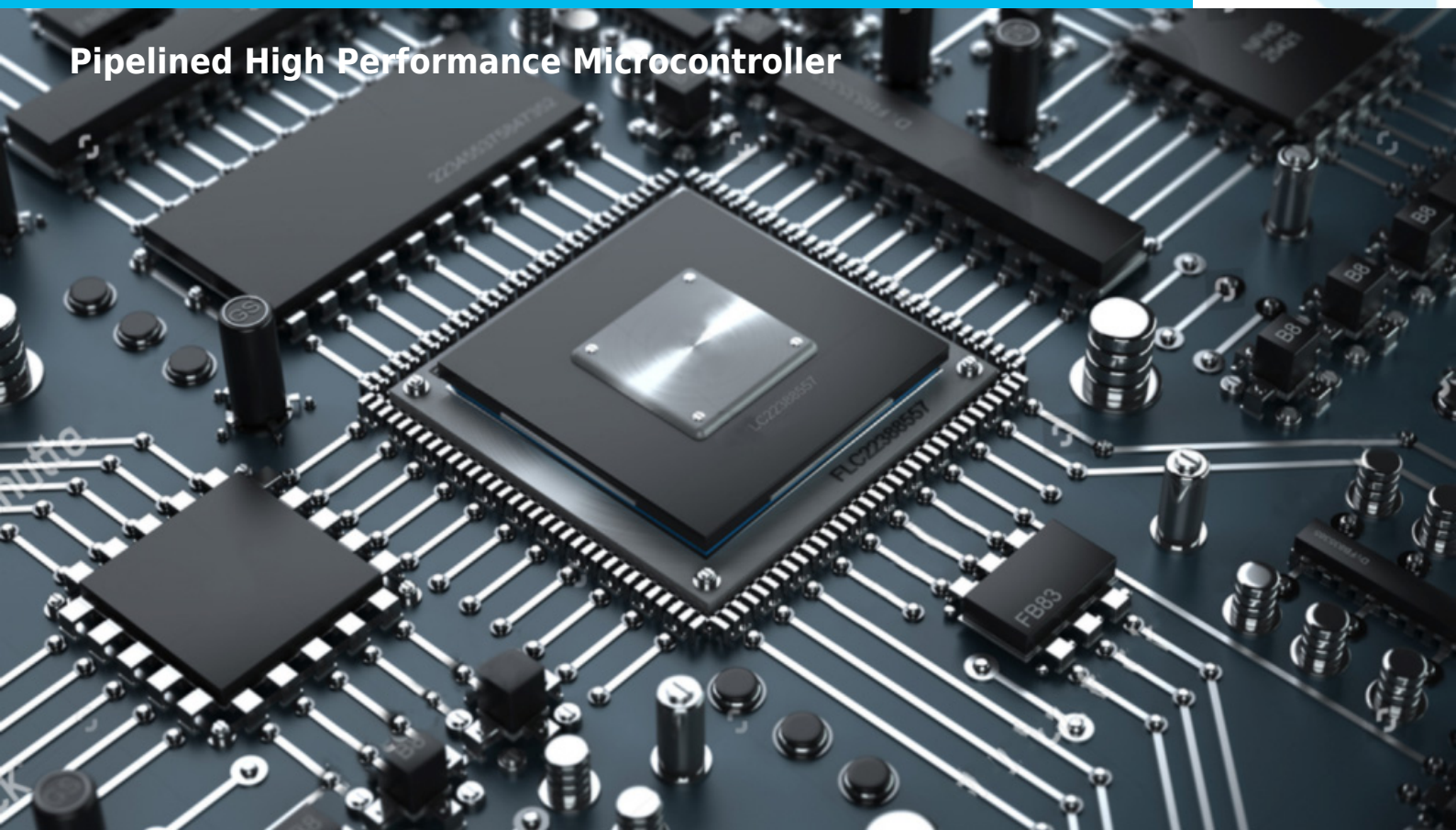
DIGITAL CORE DESIGN

DP80C51

Pipelined High Performance Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DP80C51 - IBLE HIGH-PERFOR MANCE 8051 CPU IP CORE

1 BINARY-AND PIN-COMPAT

The **DP80C51** is an **ultra-high-performance, speed-optimized 8-bit soft microcontroller IP core**, designed for **single-chip SoC implementations** that require **strict compatibility with classic 8051 devices**, while delivering **dramatically higher performance and improved power efficiency**.

Engineered to operate with both **fast on-chip memories** and **slower off-chip memory devices**, DP80C51 delivers an exceptional **performance-to-power-consumption ratio**, further enhanced by an **integrated advanced Power Management Unit (PMU)**. This makes the core ideal for **drop-in replacement designs**, **legacy system modernization**, and **long-lifecycle embedded platforms**.

FULL BINARY *AND PIN* COMPATIBILITY

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WITH CLASSIC 8051

DP80C51 is **100% binary-compatible and pin-compatible** with industry-standard **8051 8-bit microcontrollers**, enabling **seamless migration of both software and hardware designs**.

This unique compatibility allows designers to:

- Reuse **existing firmware without recompilation**
- Preserve **legacy I/O and peripheral mappings**
- Upgrade performance and power efficiency **without redesigning the board or SoC interfaces**

FLEXIBLE EXTERNAL MEMORY ARCHITECTURES

DP80C51 supports two system configurations to match different memory and bus requirements:

- **Harvard architecture** – separate external program and data buses for increased throughput
- **von Neumann architecture** – shared program and external data bus for simpler system design

This flexibility allows easy integration into **existing 8051-based memory maps** or **custom SoC architectures**.

PIPELINED RISC ARCHITECTURE WITH 10× PERFORMANCE GAIN

DP80C51 implements a **pipelined RISC microarchitecture**, delivering a **performance increase of up to 10×** compared to classic 8051 cores:

- **85–200 MIPS**, depending on configuration and operating frequency
- Significantly higher instruction throughput than standard 8051 architectures

This performance advantage can be directly converted into **power savings**. DP80C51 can be clocked **over 10× slower** than a traditional 8051 implementation while maintaining the same application-level performance — reducing **power consumption, thermal output, and EMI**.

ADVANCED POWER MANAGEMENT FOR ENERGY-EFFICIENT DESIGNS

The integrated **PMU (Power Management Unit)** enables:

- Dynamic clock scaling
- Improved performance-per-watt operation
- Reduced power dissipation in always-on systems
- Extended battery life for portable and IoT devices

These features make DP80C51 suitable for **energy-sensitive and long-term embedded applications**.

SOC-READY VERIFICATION AND NON-INTRUSIVE DEBUGGING

DP80C51 is delivered with a **fully automated testbench and a comprehensive regression test suite**, allowing **easy IP validation and integration** throughout the entire SoC design flow.

Each DP80C51 core includes built-in support for **DoCD™ (Digital Core Design on-Chip Debugger)** — a proprietary **real-time hardware debugging system** that enables **full visibility of a running SoC without disrupting application execution**.

DoCD™ Debug Capabilities

- Run, halt, single-step, step-over, and instruction skipping
- Read/write access to **all CPU registers**, **SFRs**, and **user-defined peripherals**
- Full access to **internal and external program and data memories**
- **True non-intrusive debugging** for real-time embedded systems

KEY BENEFITS FOR DESIGN ENGINEERS

- **Binary- and pin-compatible 8051 CPU IP**
- **Up to 200 MIPS** in an 8-bit architecture

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- Up to **10× performance improvement** over classic 8051
- Advanced **PMU for low-power SoCs**
- Harvard or von Neumann external memory architectures
- Fully synthesizable **ASIC & FPGA-ready soft IP**
- **Non-intrusive, real-time SoC debugging**
- Complete verification environment included

TARGET APPLICATIONS

Industrial

- Legacy industrial controllers
- Drop-in performance upgrades
- Long-lifecycle automation systems

Automotive

- Body electronics and control modules
- Automotive monitoring systems
- Mixed-signal automotive ASICs

IoT & Embedded

- Smart meters and sensors
- Battery-powered embedded nodes
- Legacy IoT platform upgrades

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

CPU FEATURES

- Pin in 100% compatible with industry standard 8051
- Software in 100% compatible with industry standard 8051
- Pipelined RISC architecture
- 10 times faster, compared to 8051 standard
- 24 times faster multiplication
- 12 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64 kB of internal (on-chip) or external (off-chip) Program Memory
- Up to 64 kB of external (off-chip) Data Memory
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- Dedicated signal for Program Memory writes
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design, with positive edge clocking and no internal tri-states
- Scan test ready
- **2 GHz virtual clock frequency** in a 0.25u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP80C51 soft core is dedicated to operate with Internal and External Program Memory. Internal Program Memory can be implemented as:

- ROM located in address range between 0x0000 ¸ (ROM_{size}-1)
- RAM located in address range between (RAM_{size}-1) ¸ 0xFFFF

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ¸ RAM_{size}.

INTERNAL DATA MEMORY:

The DP8C051 can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented, as a Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:

The DP80C51 soft core can address up to 64 kB of External Data Memory.

USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80C51 design. ESFRs are memory mapped into Direct Memory, between addresses 0x80 and 0xFF, in the same manner, as core SFRs. They may occupy any address that is not occupied by a SFR core.

WAIT STATES SUPPORT:

The DP80C51 soft core is dedicated for operation with a wide range of Program and Data memories. Slow Program and External Data memory, may assert a memory WAIT signal,

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to hold up CPU activity for required period of time.

PERIPHERALS

- **DoCD™ debug unit**
  - Processor execution control
    - Run
    - Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoint
    - one at Internal (direct) Data Memory
    - one at Special Function Registers (SFRs)
    - one at External Data Memory
  - Hardware watchpoints activated at a certain
    - address by any write into memory
    - address by any read from memory
    - address by write into memory required data
    - address by read from memory required data
  - Unlimited number of software watch-points
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Unlimited number of software breakpoints
    - Program Memory(PC)
  - Instructions Smart Trace Buffer – configurable up to 8192 levels (optional)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- **Power Management Unit**
  - Power management mode
  - Switchback feature
  - Stop mode
- **Interrupt Controller**
  - 2 priority levels
  - 2 external interrupt sources
  - 3 interrupt sources from peripherals
- **Four 8-bit I/O Ports**
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- **Two 16-bit timer/counters**
  - Timers clocked by internal source
  - Auto reload 8-bit timers
  - Externally gated event counters
- **Full-duplex serial port**
  - Synchronous mode, fixed baud rate
  - 8-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, variable baud rate

UNITS SUMMARY

Arithmetic Logic Unit – Performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. Performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C and DoCD™ module.
External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL). Performs external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States, and it allows core to work with different speed program memories.
Internal Data Memory Interface – This interface controls access into the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) by using all direct addressing mode instructions.
Interrupt Controller – Responsible for the interrupt manage system for the external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers. Please note, that external pins of this module are connected to appropriate pins of P3 port.
Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as a clock source for UARTs. Please note, that external pins of this module are connected to appropriate pins of P3 port.
UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be

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synchronized by Timer 1. Please note, that external pins of this module are connected to appropriate pins of P3 port.

Ports – Contains 8051's general purpose I/O ports. Each of port's pin can be read/written as a single bit or as an 8-bit bus P0, P1, P2, P3. The P0, P2, P3 are multi-functional ports. When used with External memory, P0 works as a multiplexed Data/LSB address to memory, and P2 works as a MSB address to external memory, P3.6 is a write signal and P3.7 is a read signal. Functionality of port is the same as in legacy 80C51 microcontroller.

Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run the core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Thee switchback feature allows UARTs and interrupts to be processed in a full speed mode, if enabled. It is highly desirable, when the microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – A **Real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, the **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by the **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with the core in a real time debugging. It is built, as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

CONFIGURATION

The following parameters of the DP80C51 core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Internal Program Memory type: *synchronous / asynchronous*
- Internal Program ROM Memory size: *0 – 64kB*
- Internal Program RAM Memory size: *0 – 64kB*
- Interrupts: *subroutines location*
- Power Management Mode: *used / unused*
- Stop mode: *used / unused*
- **DoCD™** debug unit: *used / unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following tables give a survey about the Core area and performance in **INTEL** Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed grade	F_{max}
FLEX10KE	-1	57 MHz
ACEX1K	-1	57 MHz
APEX20K	-1	50 MHz
APEX20KE	-1	66 MHz
APEX20KC	-7	78 MHz
APEX-II	-7	76 MHz
MERCURY	-5	100 MHz
CYCLONE	-6	91 MHz
CYCLONE-II	-6	93 MHz
STRATIX	-5	90 MHz
STRATIX-II	-3	160 MHz

Core performance in INTEL FPGA® devices

For the user, the most important aspect is the application speed improvement. The most commonly used arithmetic functions and their improvement are shown in the following table. The improvement was computed as {80C51 clock periods} divided by {DP80C51 clock periods} required to execute an identical function for code executed from internal (first column) and external (second column) program memory. More details are available in the core documentation.

Function	Improvement	
8-bit addition (*immediate data*)	**9,00**	**3,00**
8-bit addition (*direct addressing*)	**9,00**	**3,00**
8-bit addition (*indirect addressing*)	**9,00**	**3,60**
8-bit addition (*register addressing*)	**12,00**	**4,00**
8-bit subtraction (*immediate data*)	**9,00**	**3,00**
8-bit subtraction (*direct addressing*)	**9,00**	**3,00**
8-bit subtraction (*indirect addressing*)	**9,00**	**3,60**
8-bit subtraction (*register addressing*)	**12,00**	**4,00**
8-bit multiplication	**16,00**	**6,00**
8-bit division	**9,60**	**4,80**
16-bit addition	**12,00**	**4,00**
16-bit subtraction	**12,00**	**4,00**
16-bit multiplication	**13,60**	**5,47**
32-bit addition	**12,00**	**4,00**
32-bit subtraction	**12,00**	**4,00**
32-bit multiplication	**12,60**	**4,89**
Average speed improvement:	**11,12**	**4,03**

Dhrystone Benchmark Version 2.1 was used to measure the Core performance. The following table gives a survey about the DP80C51 performance in terms of Dhrystone/sec and VAX MIPS rating for testing code executed from external (1) and

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internal (2) program memory.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	–	12 MHz	268 (0.153)
80C310	–	33 MHz	1 550 (0.882)
DP80C51[1]	STRATIX-II	150 MHz	11 525 (6,563)
DP80C51[2]	STRATIX-II	150 MHz	26 220 (14.924)

The area utilized by each unit of the DP80C51 core in vendor specific technologies is summarized in the following table.

Component	Area	
	[LE]	[FFs]
CPU*	1 670	310
Interrupt Controller	150	40
Power Management Unit	10	5
I/O ports	100	35
Timers	160	50
UART0	210	60
Total area	**2 300**	**500**

Core components area utilization in all technologies except STRATIX-II
*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Component	Area	
	[LE]	[FFs]
CPU*	1 305	310
Interrupt Controller	115	40
Power Management Unit	10	5
I/O ports	75	35
Timers	125	50
UART0	160	60
Total area	**1 790**	**500**

Core components area utilization in STRATIX-II

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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