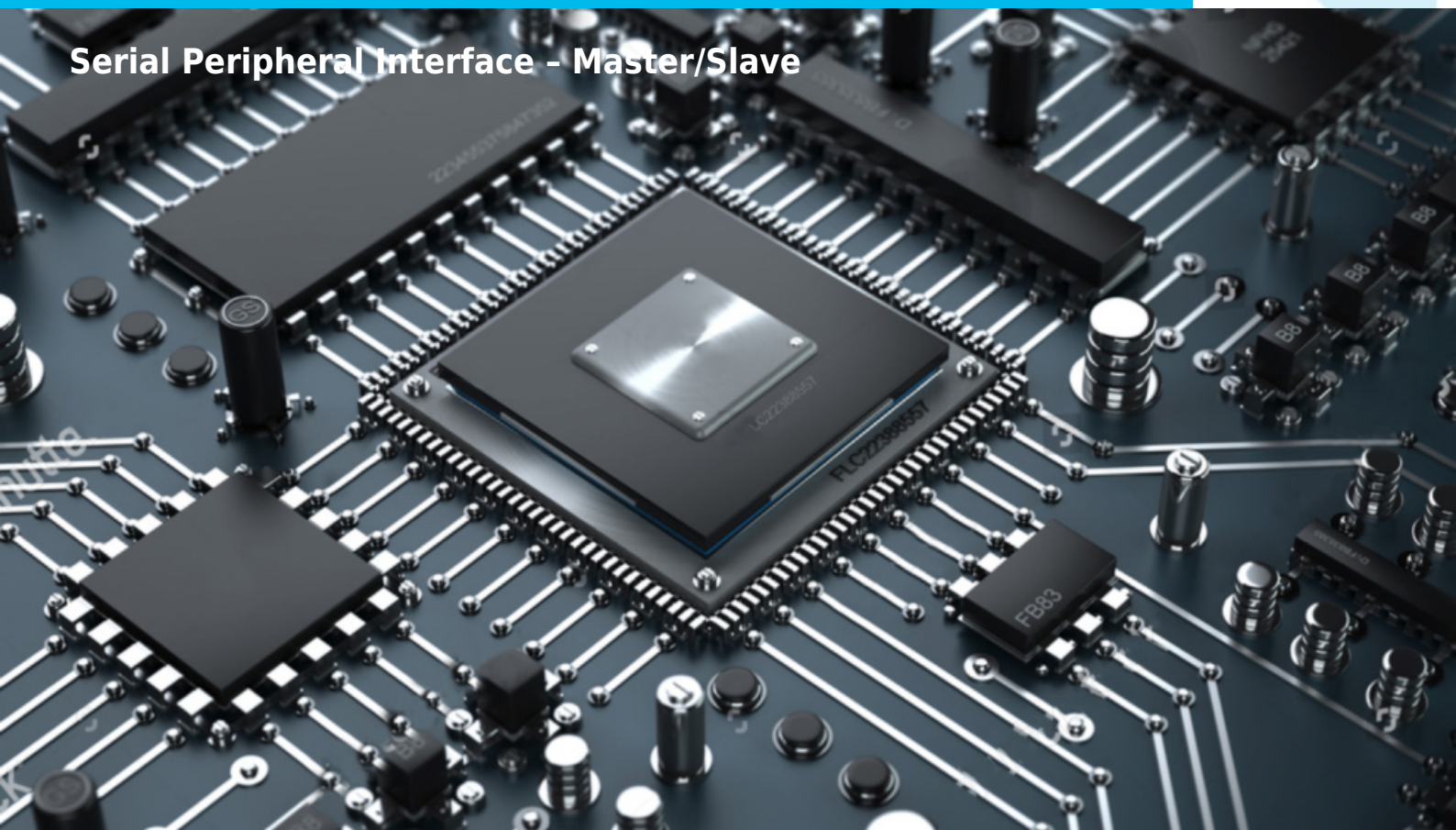
DIGITAL CORE DESIGN

DSPI

Serial Peripheral Interface – Master/Slave



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DSPI bridge to APB, AHB, and AXI bus, it is a **fully configurable SPI master/slave device**, which allows you to configure the polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also **capable of interprocessor communications in a multi-master system**. A serial clock line (SCK) synchronizes the shifting and sampling of information on two independent serial data lines. DSPI data is simultaneously transmitted and received. What's most important, it's a **technology-independent design** that can be implemented in a variety of process technologies. The DSPI system is **flexible enough to interface directly with numerous standard product peripherals from several manufacturers**. It can be configured as a master or slave device, with **data rates as high as CLK/4**. Clock control logic allows selecting clock polarity and choosing two fundamentally different clocking protocols, to accommodate the most available synchronous serial peripheral devices. When the SPI is configured as a master, the software selects one of eight different bit rates for the serial clock. The DSPI automatically drives selected by **SSCR (Slave Select Control Register) slave outputs (SS7O – SS0O)** and addresses the SPI slave device to exchange serially shifted data. What's more important, error-detection logic is included, to support interprocessor communications. A write collision detector indicates when an attempt is made to write data to the serial shift register, while the transfer is in progress. A multiple-master mode-fault detector automatically disables DSPI output drivers, if more than one SPI device simultaneously attempts to become a bus master. What does it mean for you? The **DSPI is fully customizable**, which means, that we deliver it **tailored to your configuration and requirements**. There is no need to pay extra for unused features and wasted silicon. It includes a fully automated test bench with a complete set of tests, allowing easy package validation at each stage of the SoC design flow.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- **SPI Master**
  - Master and Multi-master operations
  - 8 SPI slave select lines
  - System error detection
  - Mode fault error
  - Write collision error
  - Interrupt generation
  - Supports speeds up 1/4 of system clock
  - Bit rates generated 1/4 – 1/512 of system clock.
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- **SPI Slave**
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up 1/4 of system clock
  - Simple interface allows easy connection to microcontrollers
  - Four transfer formats supported
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

UNITS SUMMARY

SPI Clock logic – Controls phase and polarity of the SCK clock line. In the same time it detects correct sample and shift edge for the Shift register. SPI Clock Logic allows user to select any of four combinations of serial clock (SCK) phase and polarity using two pins CPHA and CPOL. The clock polarity is specified by the CPOL, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase CPHA selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPIS allows direct interface to almost any existing synchronous serial peripheral. **Shift register** – The central element in the

SPI system. When SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously moved in a second data pin. Another way to view this transfer is when an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is moved 8-bit positions. Moreover, the characters in the master and slave are effectively exchanged. **Data Register** – Holds data read from passive device, to be sent serially to the SPI Master. **Address Register** – Holds address presented on Address bus. Its contents are incremented every single data portion sent/ received serially through the SPI bus. **SPI Controller** – Detects the beginning and end of SPI transfer. Manages data exchange between DSPIS and a passive device controlled by DSPIS and increments Address Register (SPAD) after any successful transfer.

TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI, allows direct interface to almost any existing synchronous serial peripheral.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

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PERFORMANCE

The following table gives a survey about the Core performance in **INTEL FPGA®** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	F_{max}
CYCLONE	-6	79	354 MHz
CYCLONE2	-6	87	329 MHz
STRATIX	-5	79	386 MHz
STRATIX2	-3	84	422 MHz
STRATIXGX	-5	79	382 MHz
MERCURY	-5	95	347 MHz
EXCALIBUR	-1	82	224 MHz
APEX2A	-7	82	320 MHz
APEX20KC	-7	82	241 MHz
APEX20KE	-1	82	202 MHz
APEX20K	-1	82	140 MHz
ACEX1K	-1	87	196 MHz
FLEX10KE	-1	87	204 MHz
MAX2	-3	79	257 MHz
MAX3K	-5	57	114 MHz
MAX7K	-5	57	114 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy

and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

– VHDL or Verilog RTL synthesizable source code (called HDL Source code)

– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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